Aperture Array Integrated Receiver
AAIR

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General objectives

- Realization of an integrated receiver system for radio astronomy for use in dense aperture arrays.
- Frequency band and features : AA-mid
- ASIC : Next generation demonstrators
- Best compromise between :
  - Performance
  - Power consumption
  - Cost

Partnership

USN / OBSPARIS : Nançay Radio Observatory
Laboratory of Observatory of Paris

Radio Frequency components expertise & Test, Low noise amplifiers, Filters, Analog BeamFormer, Integrated Time Delay, mixers, ADC and digital circuits

LAB : Laboratory of Astrophysics of Bordeaux

Digitization expertise, ADC and digital circuits, chip packaging, electronics cards for high speed applications, digital data processing

ASTRON : Netherlands Institute for Radio Astronomy

System architecture expertise, Innovative instruments, System design, Tile antennas, test & measurement equipment

NXP : Semiconductor Industry

Manufacturing expertise, assembly & packaging, RF technology
Design Kit development, silicon process

Project cost / manpower

- ANR : Agence Nationale de la Recherche Française
  (French Research National Agency)

- Granted funding = 816 000 euros during 4 years
  [1st january 2012- 31th december 2015]

- Total permanent staff : 16 FTE during 4 years
  Total non-permanent staff : 6 FTE during 4 years with 1 PhD

Principal objectives

1. Low Noise Amplifier & Filter
2. Integrated Time Delay
3. Fast digitization

Data capture via optical fibres and processing:
Use of the latest FPGA generation
(Stratix V or Virtex 7 high speed transceivers development Board)

Low Noise Amplifier & filter

- First element in the chain (after tile antennas)
- Desired noise temperature at T0 = 50 Kelvins
- Taken into account :
  - Impedance of Vivaldi tile antennas versus frequency
  - Best compromise between Low power consumption
    Low noise temperature
    Low cost
- NXP Process : Silicon-Germanium-Carbon
- Filter integrated on chip -> System on chip : SOC

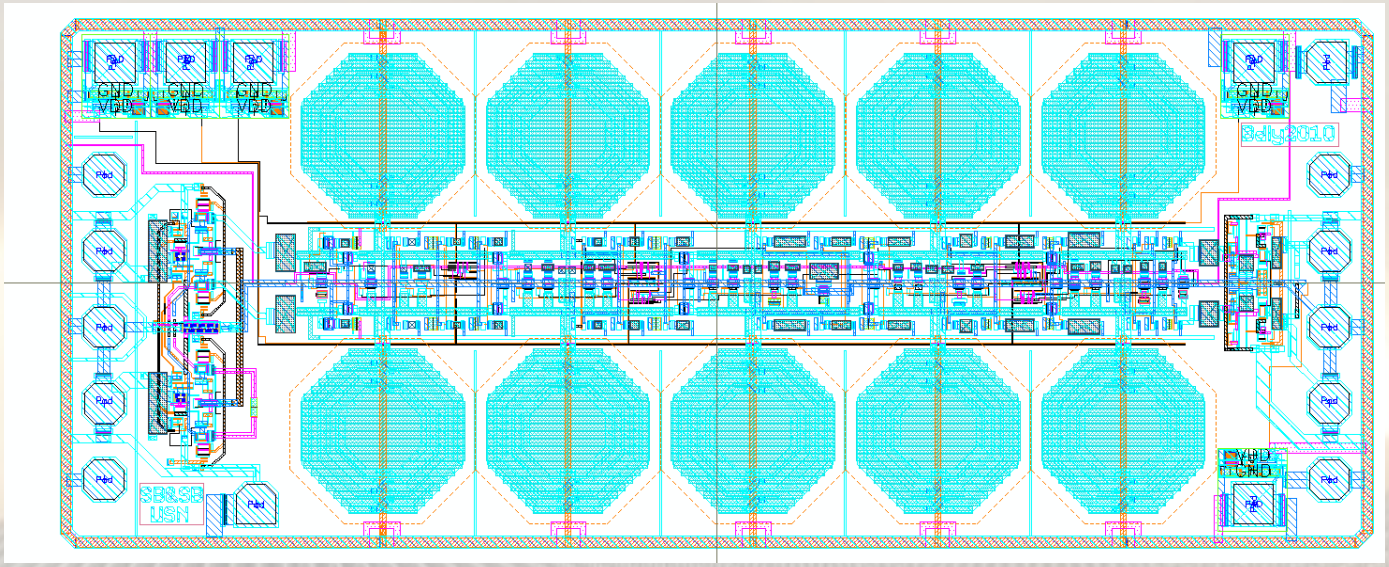
Integrated Time Delay

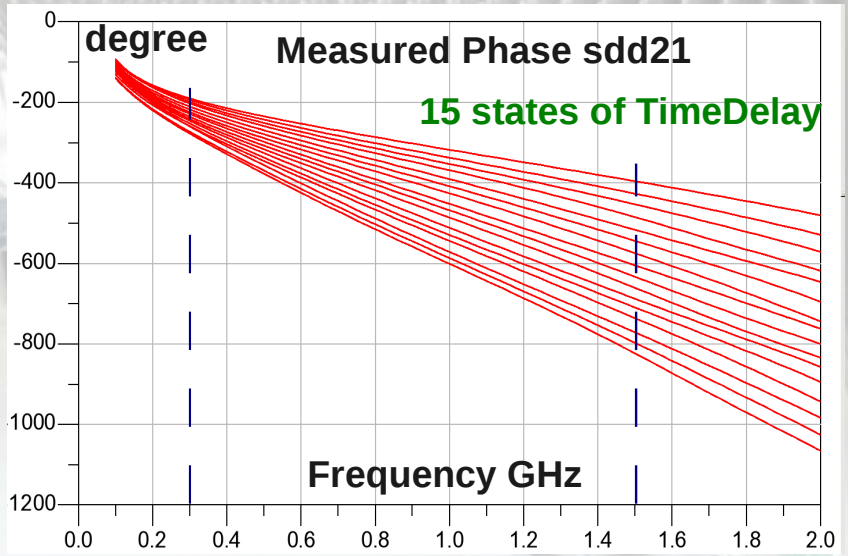
- Analog beamforming
- Integrated Phaseshifting -> Integrated Time Delay
- Use inductances and capacities
  - Reduce the power consumption
- Entire band is available for instantaneous processing
- Phase correction without « squint »
  - Improve gain of phased-array

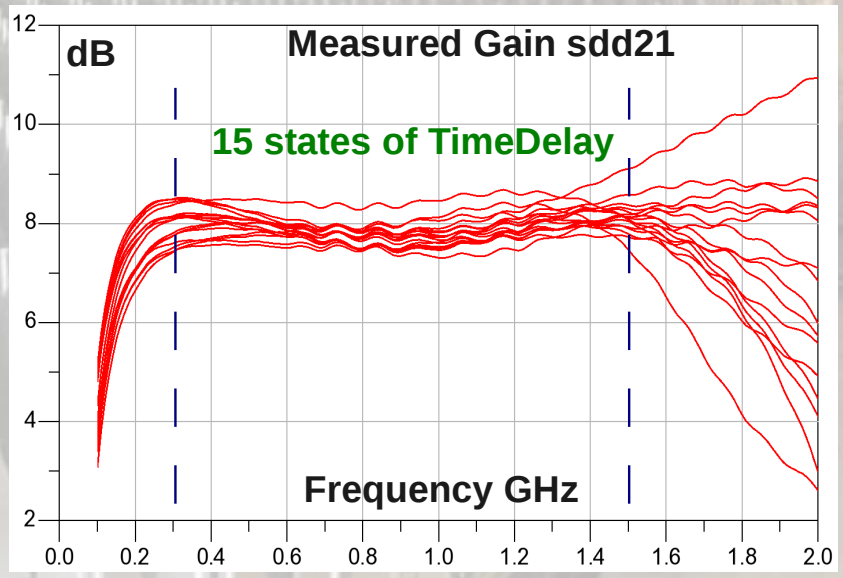
Example of integrated Time Delay

Time delay = 0.8 ns
15 step
Steps = 53 ps
Precision = ±25 ps

NXP process : Qubic4X
Surface = 2.2 mm2







Fast digitization (ADC)

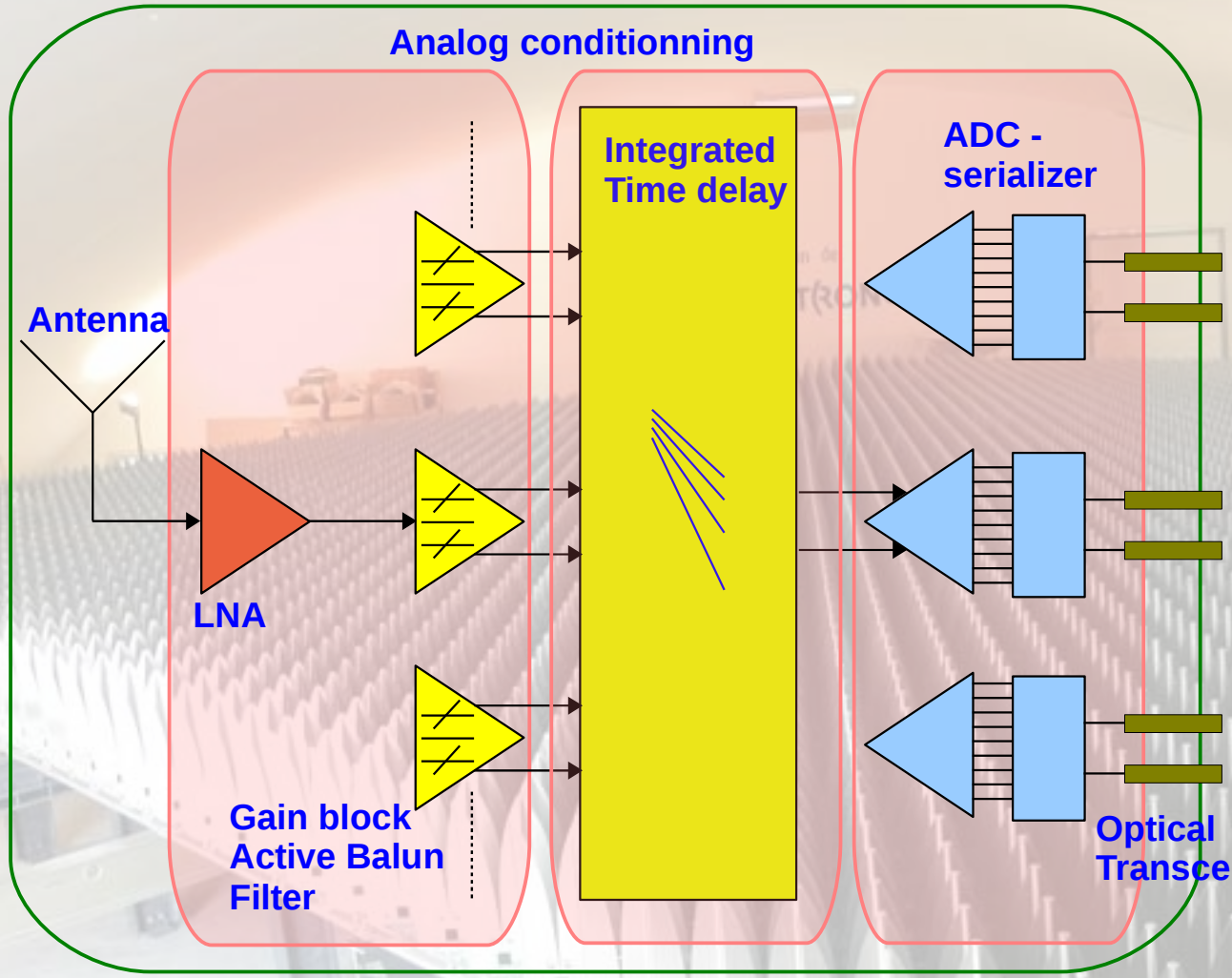
- Time delay
  - Possible elimination of mixing stage
  - ADC at the output of the tile and digitize the whole signal band
- Ultra fast ADC, pushing the current limits of the State-of-the-art
- 3 GS/s min, 8-bit resolution, ENOB > 7
- Reduction of the number components required in the receiver chain
- Silicon-Germanium-Carbon / CMOS (45nm) / Ratio

Very low cost	Very high cost	< 0.1
high consumption	Low consumption	< 2 desired

Fast digitization (serializer)

- 3 GS/s, 8-bit resolution
  - High number of Optical fibres & transceivers
- Serialization > 10 Gbits/s
  - Reduction of number of Optical fibres & transceivers
- Reduction of the cost of digital data transmission
- NXP process Silicon-Germanium-Carbon
  - Extremely fast rate : bipolar CML
  - PLL, VCO : Performance RF, jitter
- Serializer & ADC : 1 chip desired

Conclusion



2015-2016

Electronic Tile Antenna

>> Electronic EMBRACE