All hands meeting
MFAA/Receiver
Analogue-to-Digital Conversion

Stéphane Gauffre from “Université de Bordeaux”

Outline

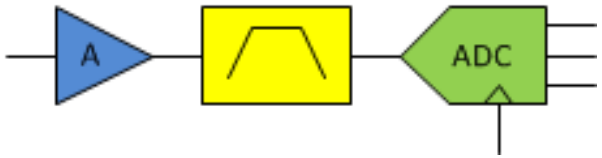
SQUARE KILOMETRE ARRAY

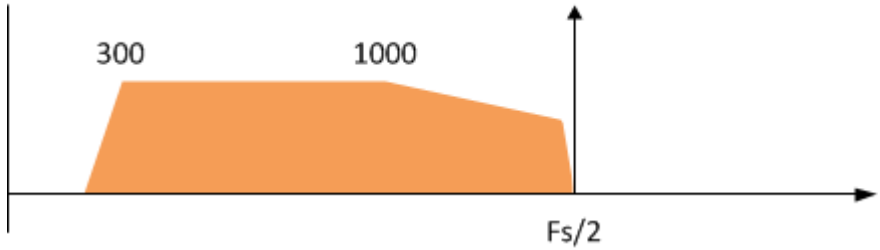
MID-FREQUENCY APERTURE ARRAY

1. Digitisation concepts for MFAA
2. Digital platform
3. Commercially available ADCs
4. Full custom ASICs solution
5. Development plan
6. Deliverables
7. Technical staff
8. Risk analysis

Digitisation concepts for MFAA

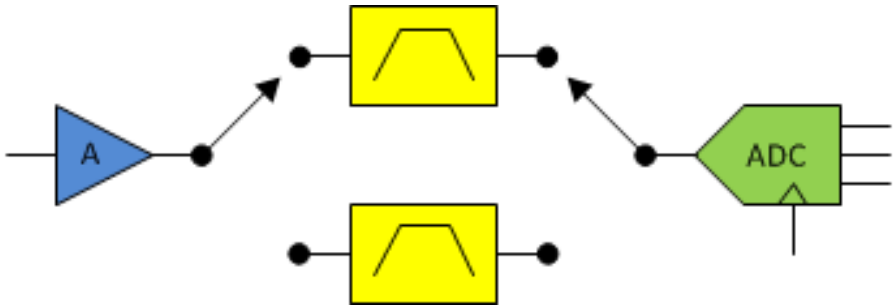
- **Wide band direct RF sampling**
  - ADC: sampling ≥ 3 GSps, bandwidth > 1450 MHz
    - First Nyquist zone

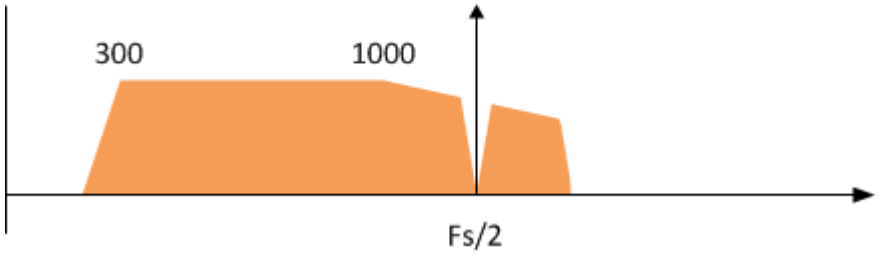




Digitisation concepts for MFAA

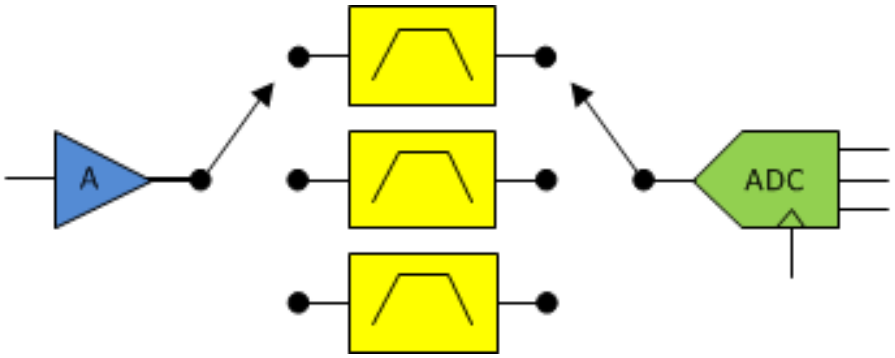
- **Direct RF sampling**
  - ADC: sampling ≥ 1.5 GSps, bandwidth > 1450MHz
    - First and second Nyquist zones
    - « Hole » around Fs/2. If Fs > 2 GSps, no « hole » in the 300-1000 MHz band.

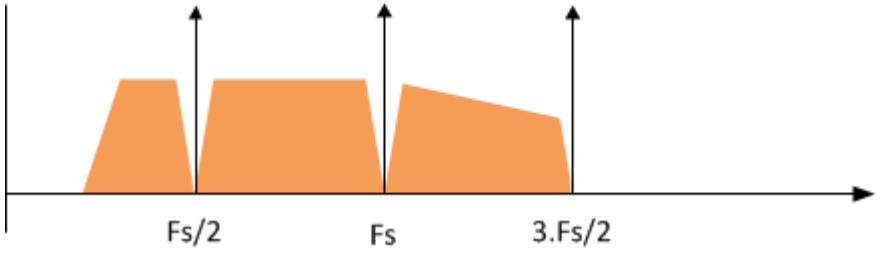




Digitisation concepts for MFAA

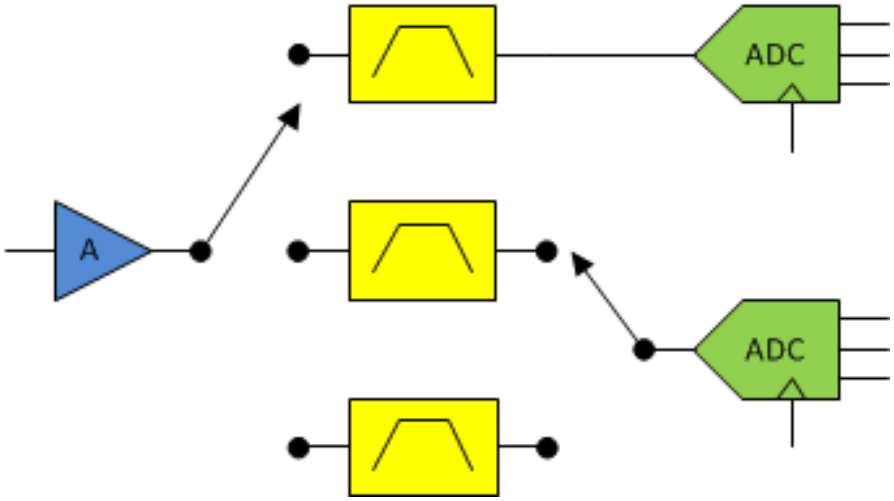
- **Direct RF sampling**
  - ADC: sampling ≥ 1 GSps, bandwidth > 1450MHz
    - First, second and third Nyquist zones
    - « Holes » around Fs/2 and Fs

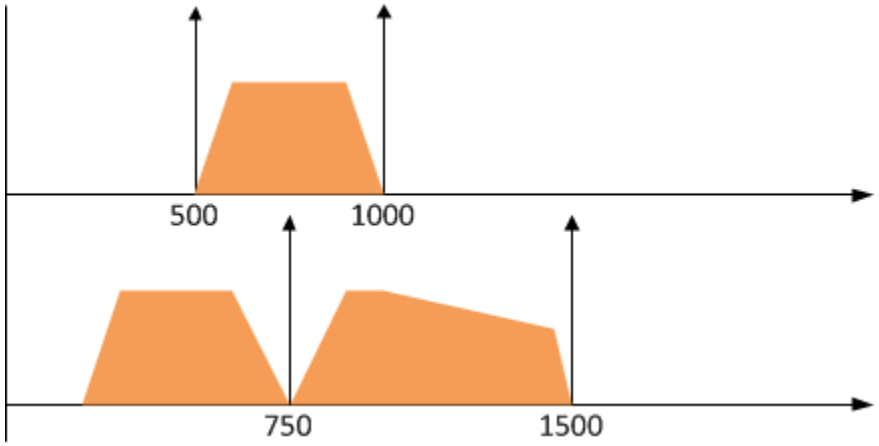




Digitisation concepts for MFAA

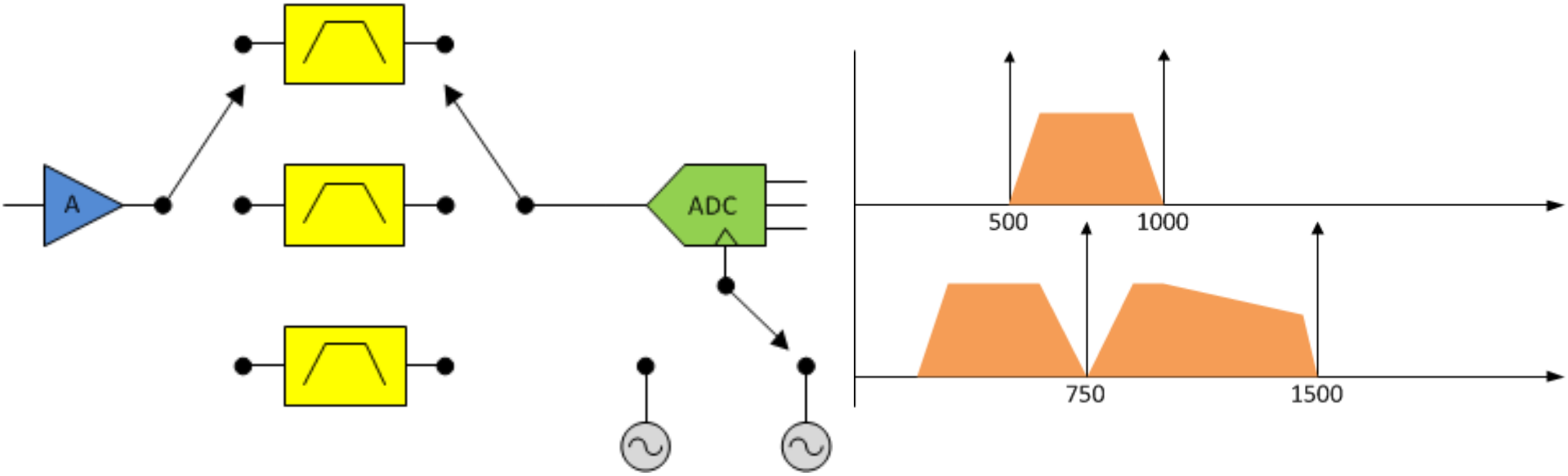
- **Direct RF sampling (bands overlapping)**
  - Use of two ADCs to have a frequency bands overlapping
    - For example: one sampled at 1 GSps, the other at 1.5 GSps





Digitisation concepts for MFAA

- **Direct RF sampling (bands overlapping)**
  - Use of 2 switched clock circuits to have a frequency bands overlapping



Digitisation concepts for MFAA

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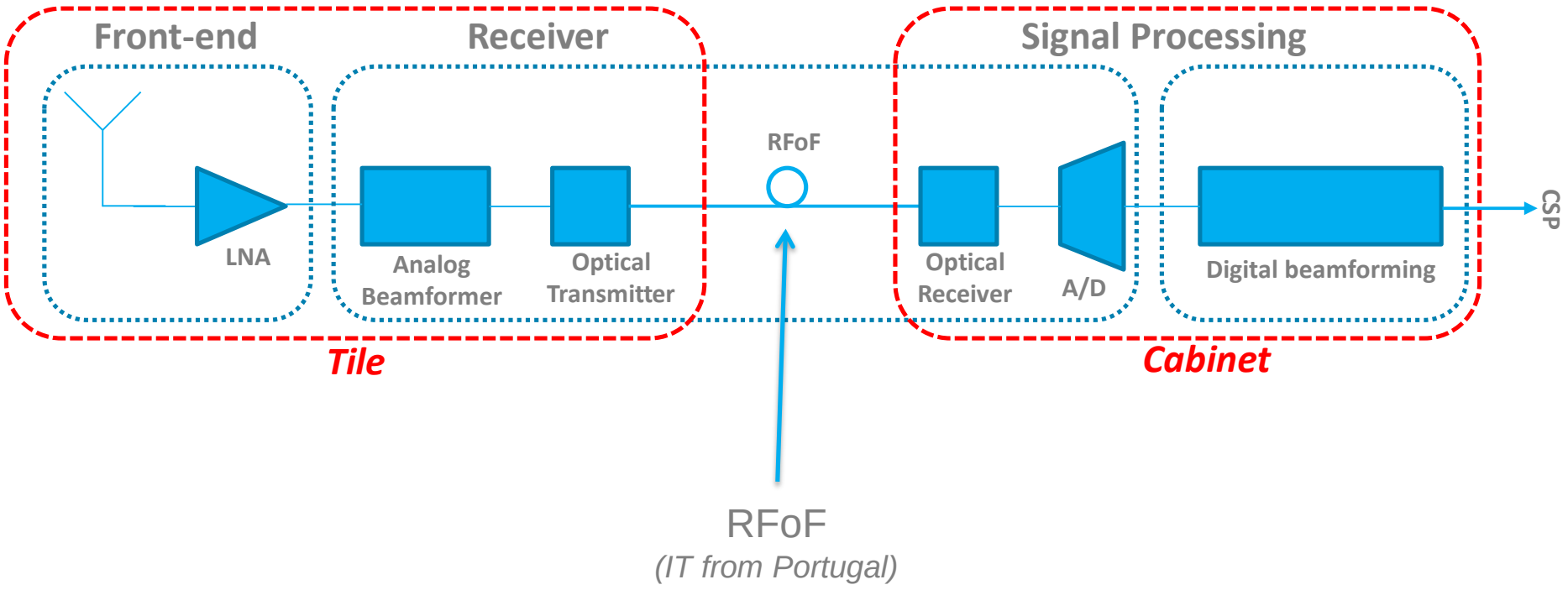
MID-FREQUENCY APERTURE ARRAY

- **Concepts comparison**

Digitisation concepts	Advantages	Disadvantages
First Nyquist zone	-Only one anti-aliasing filter **-No hole in the frequency band**	**-Highest cost** **-Highest power**
First and second Nyquist zones		**-Cost of ADCs** **-Hole in the frequency band** -2 switched anti-aliasing filters
First, second and third Nyquist zones	**-Lowest cost** **-Lowest power**	**-Holes in the frequency band** -3 switched anti-aliasing filters
Frequency bands overlapping	**-No hole in the frequency band**	**-Need two switched clock circuits** -3 or more switched anti-aliasing filters

Digital platform

- **Analog tile concept**
  - ADCs are directly connected to the digital platform



Digital platform

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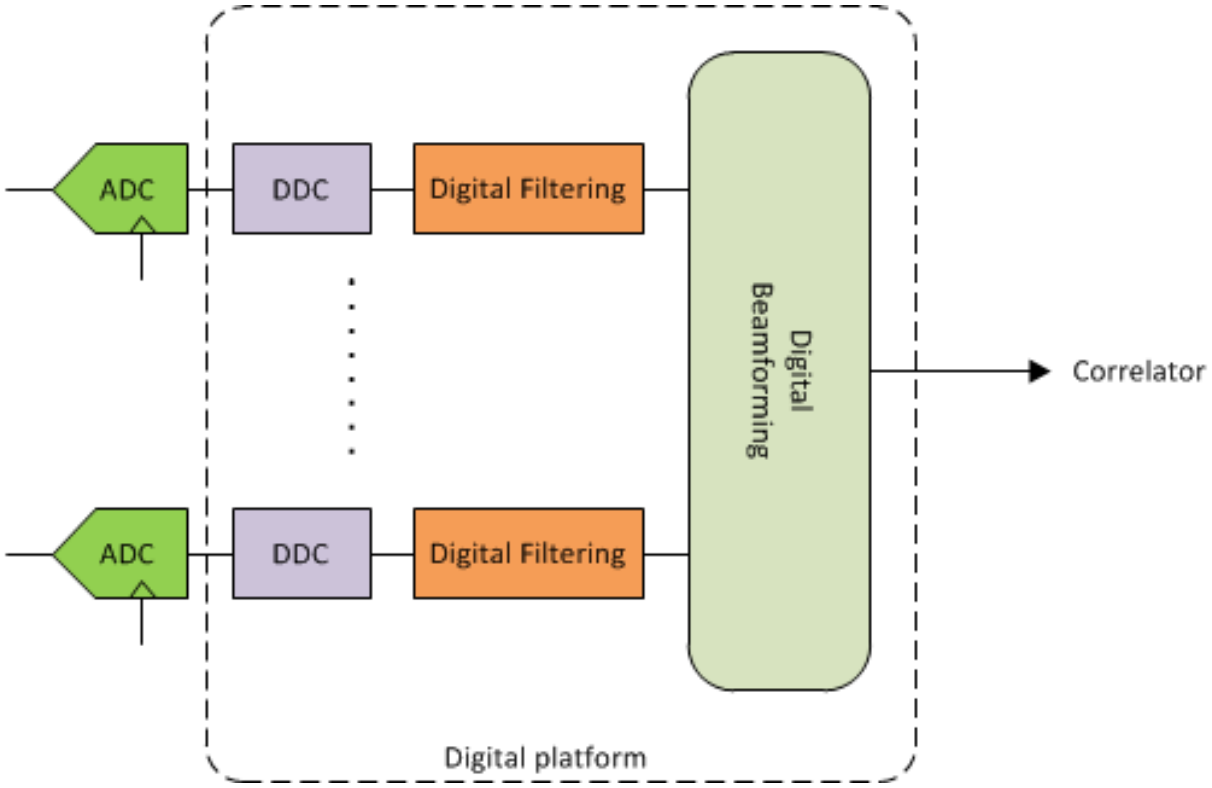
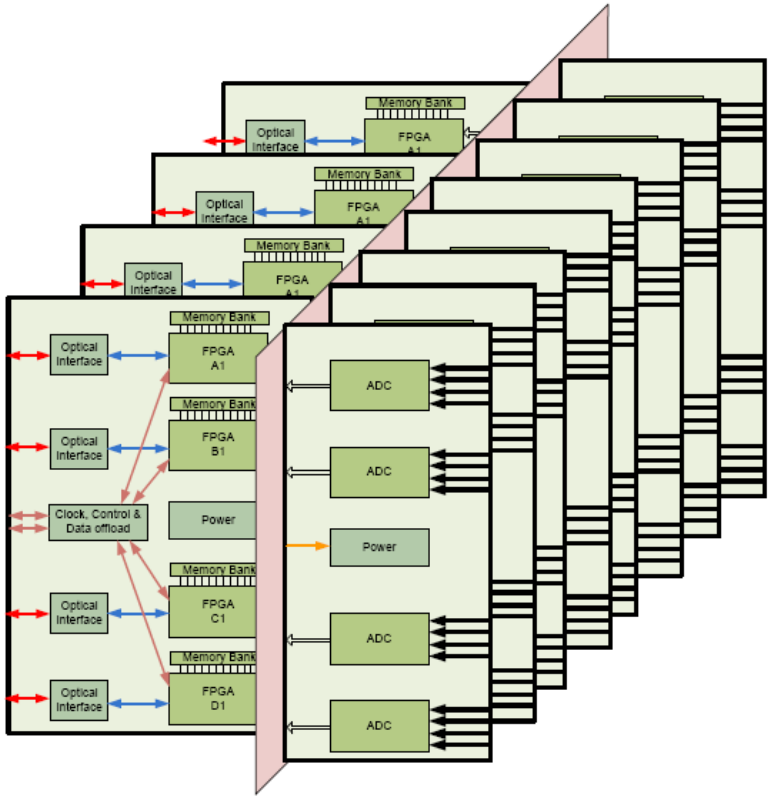


Digital platform

- **Uniboard²**
  - Multi-ADC boards connected to the BN side via special backplane
  - BN side:
    - No LVDS ports
    - JESD204B standard



Commercially available ADCs

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MID-FREQUENCY APERTURE ARRAY

Ref	Man	bit	MSps	GHz	W	Chan	Outputs	Cost	
ADC12J4000	**TI**	**12**	**4000**	**3.3**	**2.0**	**1**	**JESD204B**	**1350$**	new
ADC12J2700	**TI**	**12**	**2700**	**3.3**	**1.8**	**1**	**JESD204B**	**850$**	new
ADC12D1800RF	TI	12	1800	2.7	4.3	2	LVDS	2600€	
ADC12J1600	**TI**	**12**	**1600**	**3.3**	**1.6**	**1**	**JESD204B**	**510$**	new
ADC12D1600RF	TI	12	1600	2.7	3.9	2	LVDS	1900€	
ADC10D1500	TI	10	1500	2.8	3.6	2	LVDS	1400€	
ADC10D1000	TI	10	1000	2.8	2.8	2	LVDS	1075€	
EV10AS152A	e2v	10	3000	5.0	6.0	1	LVDS	1180€	
EV10AS150B	e2v	10	2600	5.0	6.2	1	LVDS	953€	
EV10AS180AGS	e2v	10	1500	2.25	1.8	1	LVDS	-	
EV10EQ180A	e2v	10	1250	3.2	5.6	4	LVDS	615€	
AD9680 (NDA)	**ADI**	**14**	**1000**	**-**	**-**	**2**	**JESD204B**	**-**	new
AD9625 (NDA)	**ADI**	**12**	**2500**	**-**	**-**	**1**	**JESD204B**	**-**	new
AD9234 (NDA)	**ADI**	**12**	**1000**	**-**	**-**	**2**	**JESD204B**	**-**	new

Commercially available ADCs

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MID-FREQUENCY APERTURE ARRAY

- **Evaluation of ADCs which embed the JESD204B standard**
  - ADC12J4000 (12-bit) from TI
    - Evaluation board: first results
      - Time-interleaved architecture
      - ENOB of 8 at 3 GSps
    - Engineering sample
    - Production for Q3 of 2014

Commercially available ADCs

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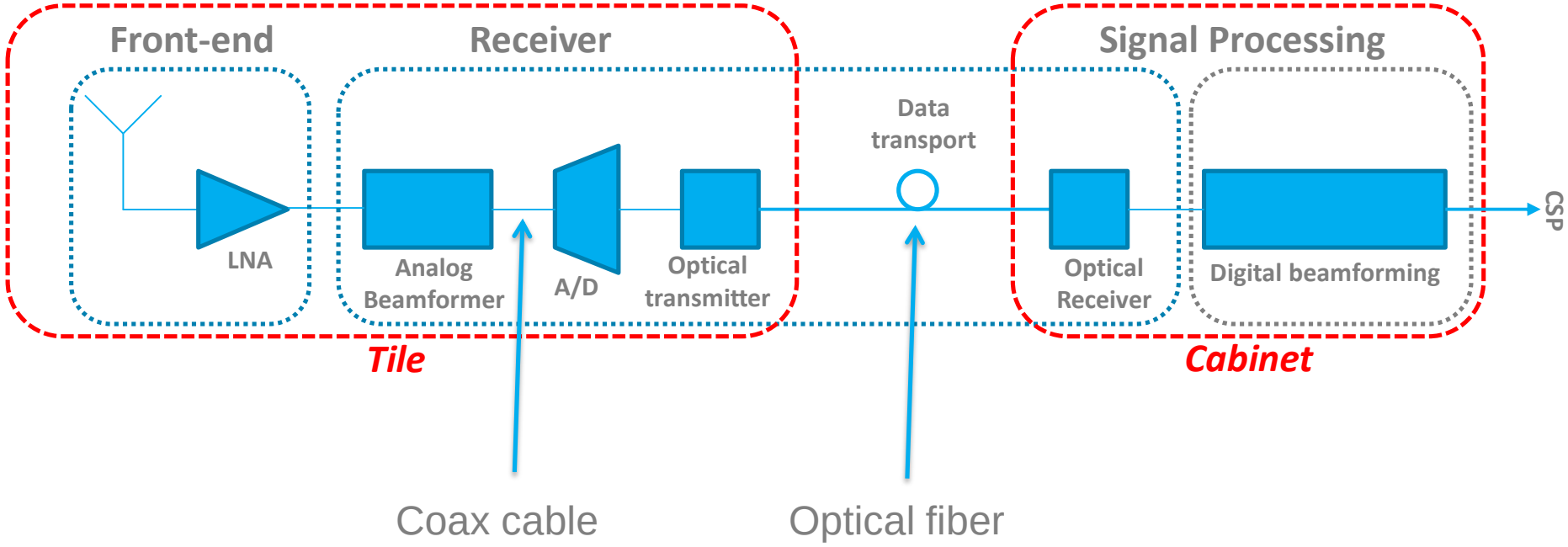
MID-FREQUENCY APERTURE ARRAY

- **Evaluation of ADCs which embed the JESD204B standard**
  - ADCs from ADI (next month)
    - AD9625 (12-bit): time-interleaved architecture?
      - Sampling at 2.5 GSps
    - **AD9234 (12-bit)** or AD9680 (14-bit):
      - Possible common multi-ADCs board for both AA.
        - ❑ 2 switched clocks: one at 1 GSps, the other at 750 MSps
        - ❑ 4 switched anti-aliasing filters: 400-600 MHz, 600-900 MHz, 900-1100 MHz and 1100-1450 MHz for MFAA
        - ❑ For LFAA: one clock at 1 GSps, one filter (50-350 MHz)
    - Contact with ADI guys (evaluation boards required)
    - Components and datasheets available before mid-2014.

Full custom ASICs solution

- **Developed in the framework of AAIR project**
  - All ASICs in 250nm BiCMOS from NXP
- **Digital tile concept**



Full custom ASICs solution

- **ADC associated to a serializer circuit to reduce digital optic links between antenna and bunker (digital platform)**
  - 8-bit, 3.5 GSps, flash folding and interpolating ADC (<1W)
    - Modeling is in progress (ENOB > 7.3 at 3 GSps)
    - Will be sent to NXP foundry in October 2014

Full custom ASICs solution

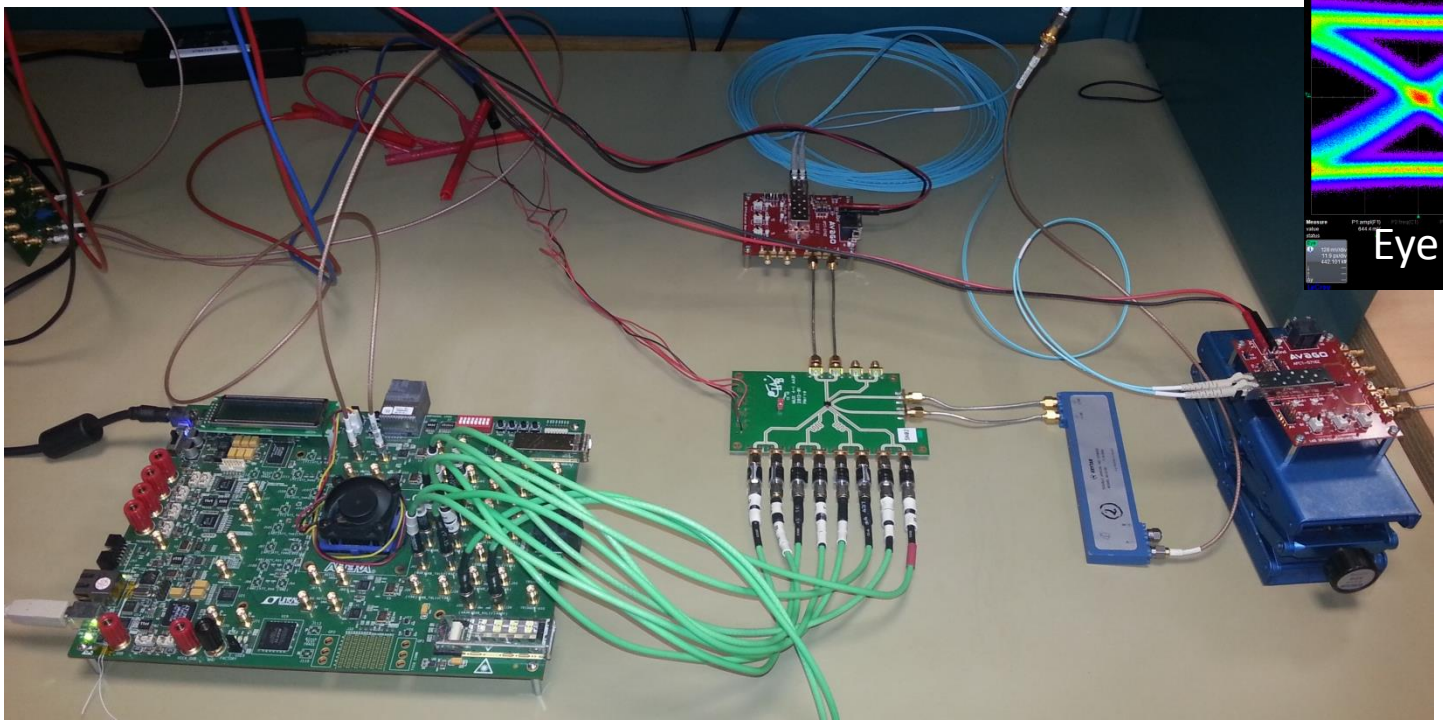
- 8 to 2 serializer circuit at 14 Gbps (1W)
  - 4 to 1 serializer circuit at 14 Gbps: already validated
  - The PLL at 7 GHz, which drives the serializer was received in January 2014. Its characterisation is in progress.
  - 8:2 serializer circuit without PLL will be sent to NXP foundry in April 2014
  - The complete serializer circuit will be sent to NXP foundry in October 2014

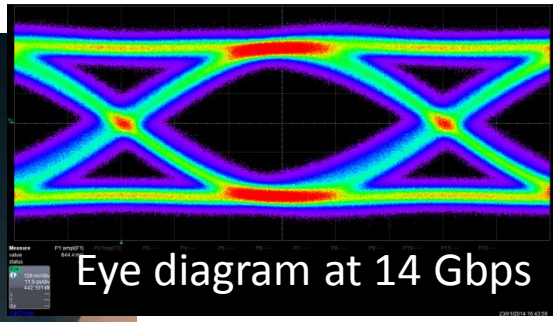
Full custom ASICs solution

SKA SQUARE KILOMETRE ARRAY

MID-FREQUENCY APERTURE ARRAY

- **First results: 4:1 serializer circuit associated to a 16 GFC optical link**

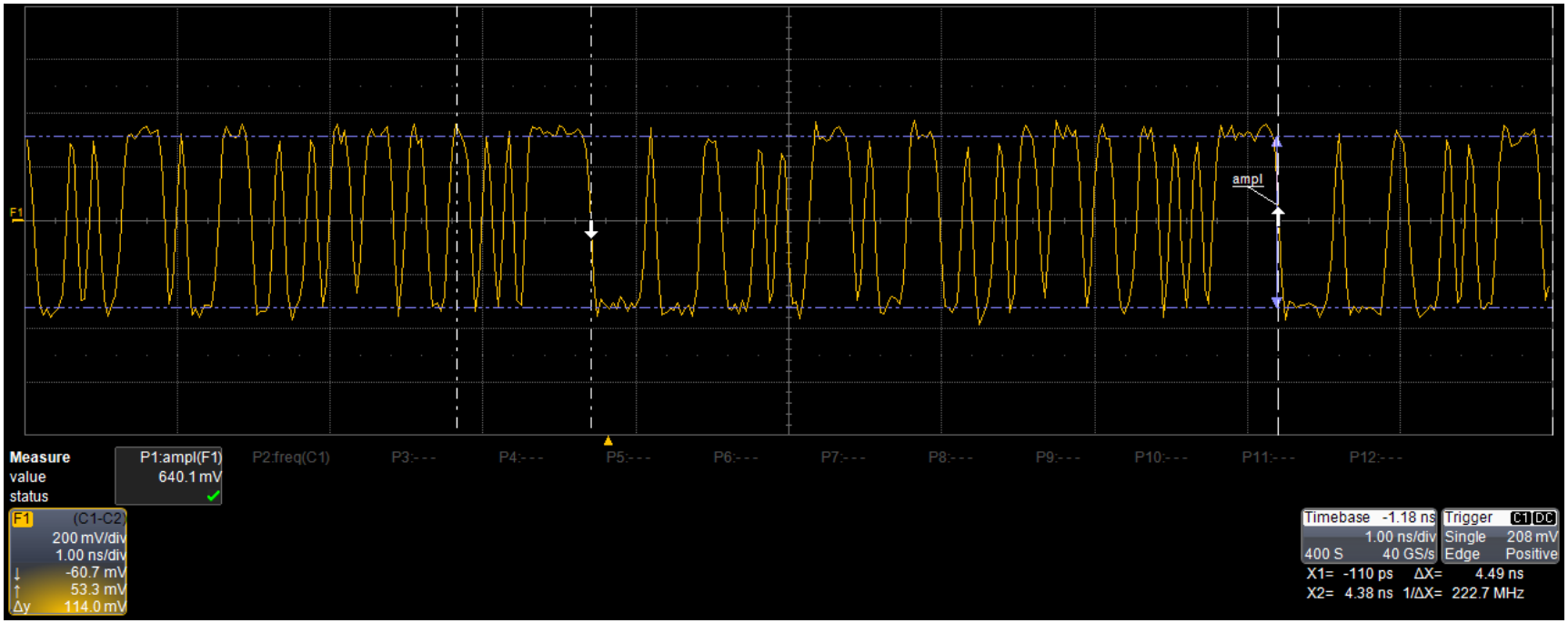




Eye diagram at 14 Gbps

Full custom ASICs solution

- **First results: 4:1 serializer circuit associated to a 16 GFC optical link**
  - PRBS7: correct bit sequence at 14 Gbps

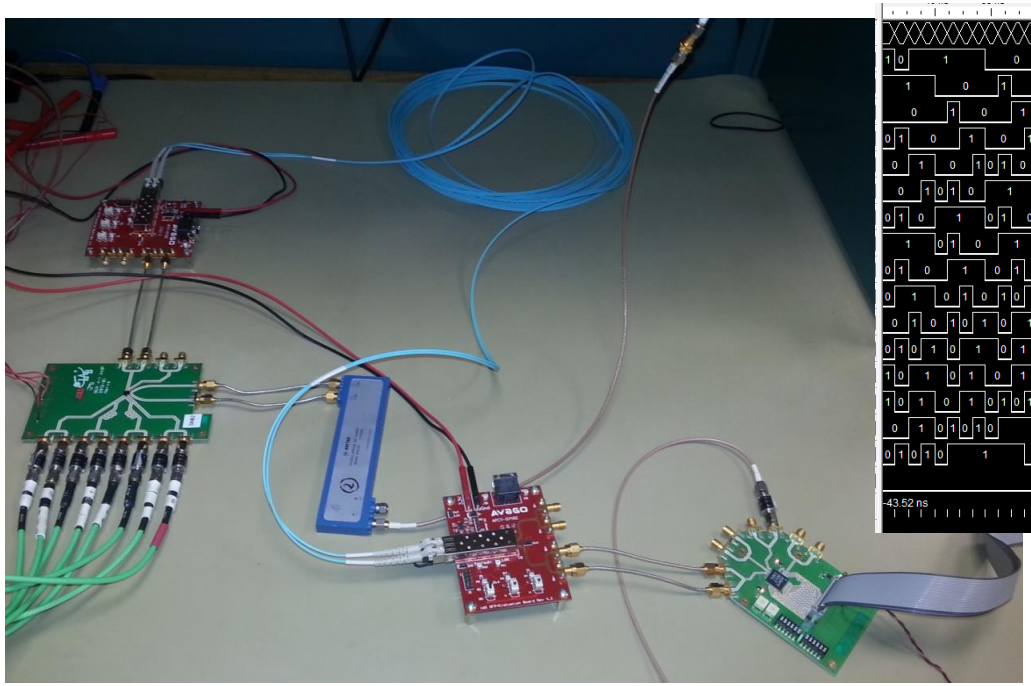


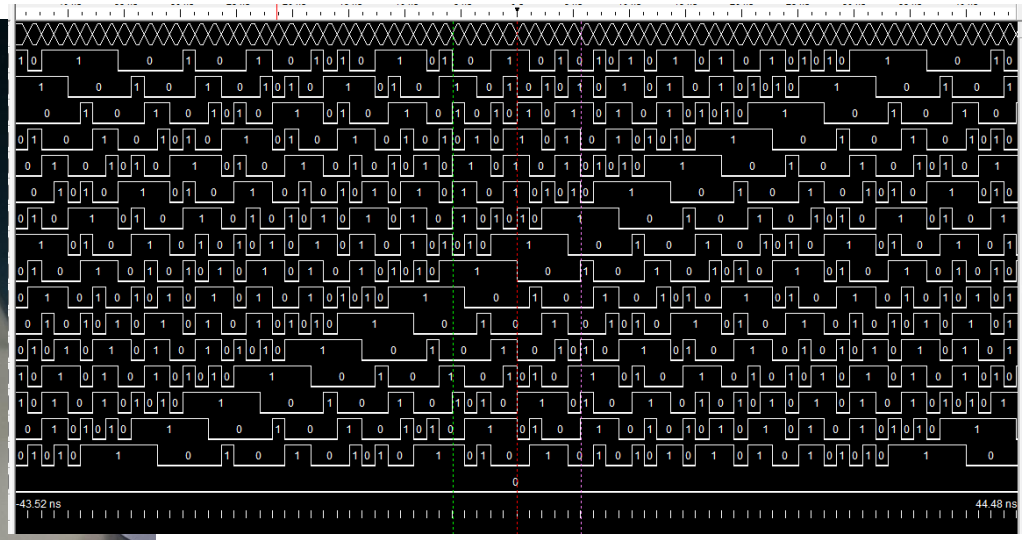
Full custom ASICs solution

SKA SQUARE KILOMETRE ARRAY

MID-FREQUENCY APERTURE ARRAY

- **First results: 4 to 1 serializer circuit associated to a 16 GFC optical link**
  - Data demultiplexed by 16 to connect to Uniboard1





Development plan

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MID-FREQUENCY APERTURE ARRAY

- **Analogue tile concept: Commercially available ADCs**
  - Selection: May or June 2014
  - First ADC board prototype: connected to Stratix5 GX development kit
    - Manufacturing in September 2014
    - Characterisation in Q4 of 2014
  - First multi-ADCs board prototype (Uniboard²):
    - Manufacturing in Q1 of 2015
    - Characterisation in Q2 of 2015

Development plan

- **Digital tile concept (AAIR project): Full custom ASICs**
  - Flash folding and interpolating ADC and 8:2 serializer circuit
    - manufacturing in Q4 of 2014
    - Characterization in Q1 of 2015
  - Digitisation board and digital board (Uniboard or Uniboard²)
    - Manufacturing in Q3 of 2015
    - Characterisation in Q4 of 2015

Deliverables

- Digitisation concepts description for MFAA
- Evaluation report for commercially available ADCs (analog tile concept)
- Evaluation report for digital data transfer via optical fiber (digital tile concept)
- Design reports for full custom ASICs (ADC and serializer circuit)
- Test reports for full custom ASICs
- Interface control document

Deliverables

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MID-FREQUENCY APERTURE ARRAY

- Design reports for electronics cards (multi-ADCs board, digitisation board and digital interface board)
- Test reports for electronics cards
- Reliability and maintenance analysis report
- Risk analysis report
- Cost estimation report for production

Technical staff (key persons)

- **Stéphane Gauffre from U. Bordeaux**: ADC task leader, permanent position
  - ASIC and PCB designer
- **Benjamin Quertier from U. Bordeaux**: Head of electronics laboratory of LAB, permanent position
  - Expert in digital electronics
- **Bruno Da Silva from O. de Paris**: permanent position
  - ASIC designer (full custom ADC)
- **Antsa Randriamanantena from U. Bordeaux**: recruited for 2 years
  - Expert in digital electronics
- **Hermann Andriantafika from U. Bordeaux**: Ph.D Student
  - ASIC designer (serializer circuit)

Risk analysis

- **Full custom ASICs could not meet the specifications.**
  - Develop a solution with COTS. Evaluation of commercially available ADCs
- **Our development plan depends on NXP foundry schedule. Some deliverables could be delayed for full custom ASICs solution.**
  - Develop a solution with COTS.

Risk analysis

- **The ADC will be associated to logic components (FPGA) and to a clock circuitry (PLL). These components generate spurious frequencies which could pollute the analogue signal.**
  - A simple shielding box is not sufficient to minimize the Radio Frequency Interference. Careful design should be done for RFI mitigation: placement and shielding of critical components, power supply decoupling.
- **Manpower is limited. This could add delays in the schedule**
  - The Key persons have permanent positions
  - A work redistribution should be done to minimize delays.