

MID-FREQUENCY APERTURE ARRAY

# All hands meeting MFAA/Receiver update

#### **G.Kenfack**

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# MFAA consortium



- 1. ASTRON
- 2. Observatoire de Paris (Nancay)
- 3. University of Bordeaux
- 4. University of Cambridge
- 5. University of Manchester
- 6. University of Oxford
- 7. KLAASA
- 8. UoMalta
- 9. Associate members:
- Spain, Portugal
- South Africa

# **MFAA** Integrated receiver



- SKA.TEL.MFAA.RE- Integrated Receiver
- Description of Work:

The main objective : To design an integrated receiver primarily to support a digital tile. To find the optimal compromise between performance, power consumption and cost the focus is on ASIC SiGe technology for the integrated receiver.

Committed resources

Participant Name	ASTRON	Obs de Paris	Université Bordeaux 1
M. months S1	4	92	84
M. months S2	2	34	24
Material			
TOTAL			

## **MFAA : RF Specifications**



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- **300-1000** MHz (AAMID-TEL.MFAA.SE.MGT-AAMID-PL-002, « Technical Description »)
- **400-1450** MHz (WP2-015-.020.010-SRS-001, « AA-mid system requirements specification »)
- AAIR project: 400-1500 MHz

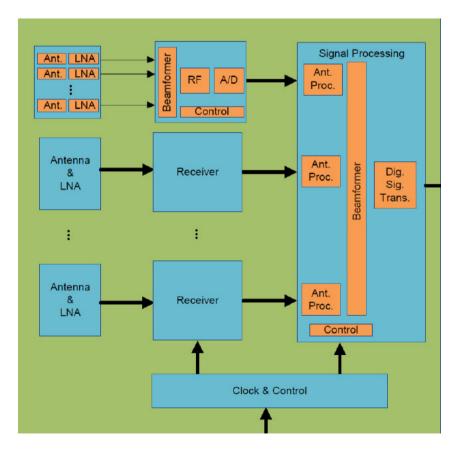
→ [ 300 – 1500 ] MHz : Best case

# Receiver Architecture1 : Digital tile

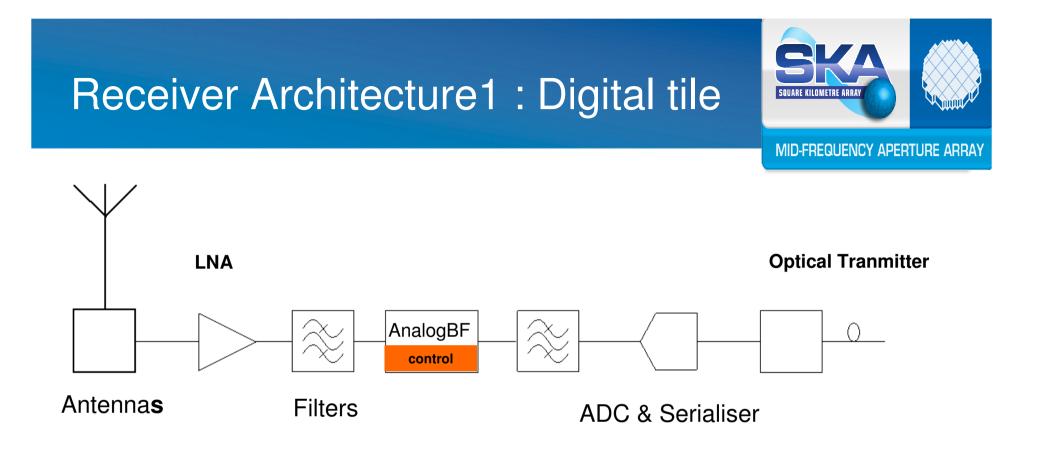


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### > ASICs & Key elements for the digital tile



- Antenna (ASTRON) : Vivaldi (single ended)
  → [450 1500] MHz
- LNA : Noise/Cost performance of bipolar SiGeC. (Located on the feedboard.)
- Filters :
  - for the RF chain : Band pass & low pass.
  - And filters for the diplexing RF and control.
- Analog Beamformer : Timedelay or phaseshifting
- Control & monitoring : I<sup>2</sup>C,SPI, low speed ADC
- ADC : flash folding , 8-bit, 3.5 GSps ADC (BiCMOS)
- Serialiser : Data up to 14 Gbps



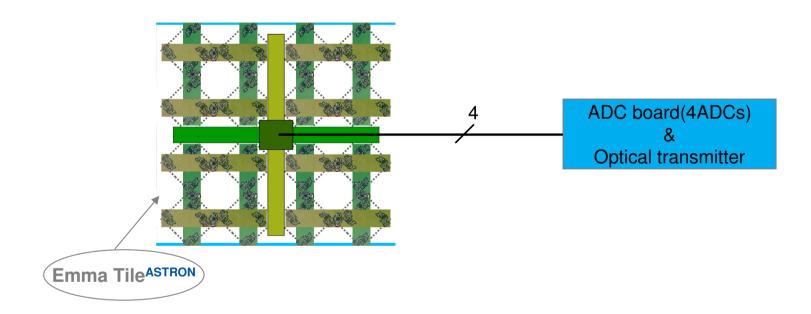
#### Single array of Tiles (Tile architecture) :

- EMMA like with 1 ADC per tile per polar per beam. ( $\rightarrow$ More flexible for the FoV)
- 32 Antennas per polarisations
- Each AnalogBF can process 4 antenna, and deliver 2 Beams on the Octoboard.
- 1 Tile = 8 octoboard per polarisation = 4 ouput Tiles available on each center board
- The 4 RF ouputs tiles (2beams, 2polar) are digitised from the Center board  $\rightarrow$  4 ADCs.

### Receiver Architecture1 : Digital tile



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### Architecture to evaluate later...



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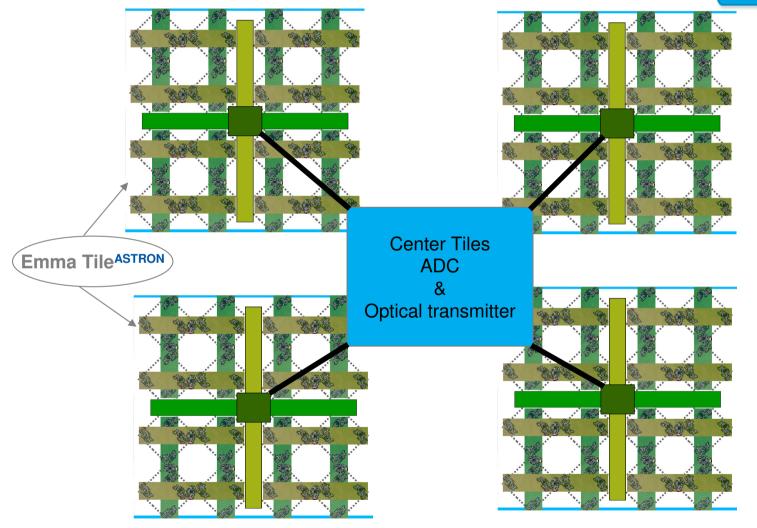
#### Tile array Summation architecture :

- EMMA like with *optimised configuration* in order to find the best trade-off between the power comsumption per channel(number of Analog BF) and the number of ADC.
- Less flexibe for the FoV
- Each AnalogBF can process 4 antenna, and deliver 2 Beams on the Octoboard.
- Another Analog Beam Forming stage on the center board with combiTiles allows the summation of 4 Tiles.
- The ouputs are digitised from the Center Tile.

### **Tile array Summation architecture**



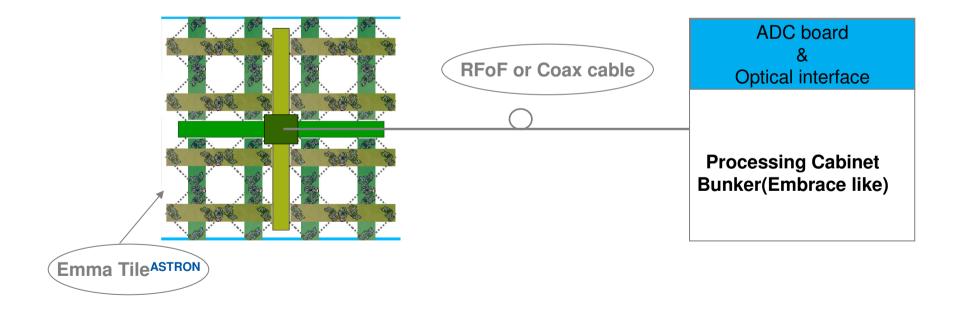
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# Receiver Architecture2 : Analog tile



- Due to RFI consideration, the ouputs are digitised at the Processing Cabinet
- 4 RF cable are used to transport the signal from the Center Tile to the Processing Cabinet.
- ADCs & Serialisers are located within the processing cabinet
- This concept(Analog Tile) will be studied in depth with cable or RFoF(see S.Gauffre talk)



### **Receiver : task description**

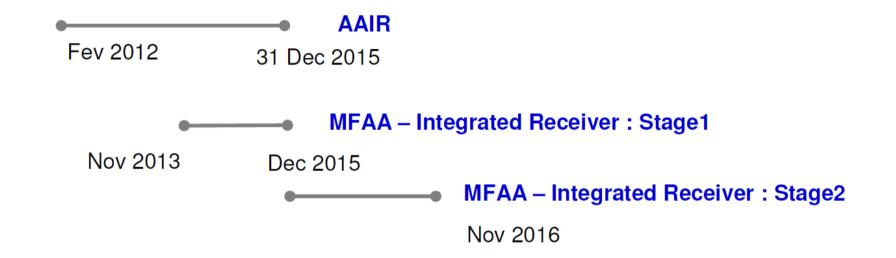


- ≻Task leader G.K
- SKA.TEL.MFAA.RE.MGT Receiver Management S.Bo
- > SKA.TEL.MFAA.RE.AE Analogue Electronics S.Bo
- > SKA.TEL.MFAA.RE.ABF Analogue Beamforming S.Bo
- SKA.TEL.MFAA.RE.ADC Analogue to Digital Conversion S.G.
- > SKA.TEL.MFAA.RE.RC Receiver Control S.Ba
- SKA.TEL.MFAA.RE.PPE Prototype and Performance Evaluation B.C

### MFAA FR : Deliverable & Milestone



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# MFAA FR : Deliverable (1)



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*Task:* Level 4 SKA.TEL.MFAA.RE – Integrated Receiver *Task leader* G. Kenfack

- 1. Integrated receiver requirements (level 5)
- 2. Integrated receiver design document (level 5)
- 3. Integrated receiver validation document (level 5)

*Task:* Level 5 SKA.TEL.MFAA.RE.MGT – Receiver-Management *Task leader* S. Bosse

- 1. System specifications of all ASICs
- 2. Simulation RF of System, including electronic RF beam diagram
- 3. Prototype synchronisation system
- 4. Study of calibration RF of one tile

# MFAA FR : Deliverable (2)



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*Task:* Level 5 SKA.TEL.MFAA.RE-AE – Analogue-Electronic *Task leader* S. Bosse

#### Deliverables:

- 1. LNA design on silicon optimised for active antenna source impedance
- 2. Filter design on silicon
- 3. Active Balun on silicon
- 4. Verification plan & test report

*Task:* Level 5 SKA.TEL.MFAA.RE-ABF – Analogue-Beamforming *Task leader* S. Bosse

### Deliverables:

- 1. Prototype ASIC Beamformer with phase-shifting
- 2. Prototype ASIC Beamformer with Time-delay
- 3. photonic aperture array beamforming system
- 4. Verification plan & Test report

# MFAA FR : Deliverable (3)



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*Task:* Level 5 SKA.TEL.MFAA.RE-RC – Receiver-Control *Task leader* S. Barth *Deliverables:* 

- 1. report on control protocols at different levels
- 2. software driver
- 3. evaluation report on RFI from tile control
- 4. ADC IP for monitoring

*Task:* Level 5 SKA.TEL.MFAA.RE.PPE – Prototype and Performance Evaluation

Task leader B. Censier

### **Deliverables:**

- 1. Integrated receiver prototype
- 2. Integrated receiver verification document

# MFAA FR : Deliverable (4)



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# *Task:* Level 5 SKA.TEL.MFAA.RE-ADC – Analogue-to-Digital Conversion *Task leader* S. Gauffre

### Deliverables:

- 1. Digitisation concepts description for MFAA
- 2. Evaluation report for commercially available ADC (analog tile concept)
- 3. Evalution report for digital data transfer via optical fiber (digital tile concept)
- 4. Design reports for full custom ASICs (ADC and serializer circuit)
- 5. Test reports for full custom ASICs
- 6. Interface control document for each concept
- 7. Design reports for electronics cards (Digitisation board and digital interface board)
- 8. Test reports for electronics cards
- 9. Reliability and maintenance analysis report
- 10. Risk analysis report
- 11. Cost estimation report for production

# **MFAA** Integrated receiver



- SKA.TEL.MFAA.RE- Integrated Receiver
- Committed resources and funds : Nov2013-Dec2015

Participant Name	ASTRON	Obs de Paris	Université Bordeaux 1
M. months S1	4	92	84
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Material			
TOTAL			

 Funding agencies: CNRS, INSU, ANR, Observatoire de Paris, LAB



### MFAA FR : identified risk

Owner	Level	Identified Risks (Notes)	Agreed Actions	Agreed Mitigations
S.BOSSE	4	Definition of analog input bandwith is not clear. [300-1000]MHz ; and there are some RFI issues around 300Mhz.	we will have to clarifiy it with A.Gunst & J.Geralt	we will provide the RF conditionning to work within this RF band[400-1500]MHz
S.BOSSE	4	The man power is limited for some design tasks, therefore some deliverables could be delayed.	the work could be done with expected high delay for the delivery.	some chips could be replaced by external COTS(commercial ADC, Serializer, monitoring).
S.BOSSE	4	Silicium technology SiGeC is mature but constantly evolving, and the		Photonic BF : to be asked to ASTRON
S.BOSSE	4	Some Designer have not permanent position, especially on Low Noise Amplifier. The risk is to lose competences which could largely delay some deliverables.	A request for permanent position will be made to our institutes.	Redistribution of task to permanent members of staff. This will affect the overall schedule.
S.BOSSE	4	The requirements could not be met for the lowest frequencies (<400MHz) like ASIC delay beamformer (stage 1). Also the performance of the vivaldi antenna at lower frequencies need to be improved.	design (stage 2)	we should look if we can improve our BFC at lower frequencies . We will work closer with Astron(Vivaldi) and Manchester(ORA).
			Exploring the Universe with the	world's largest radio telescope

### MFAA FR : Progress summary



- Progess update :
  - List of the current work progress
  - *MFAA\_RE\_work\_progress\_Jan\_march2014-FR.xlsx*