ASTRON Netherlands Institute for Radio Astronomy

SKA SQUARE KILOMETRE ARRAY MID-FREQUENCY APERTURE ARRAY

Vivaldi arrays ‘Towards SKA 2025’

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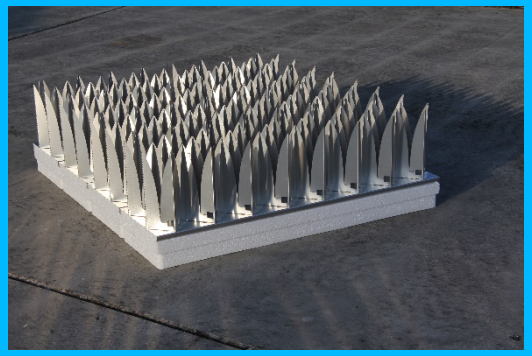
ASTRON AAMID workpackage leader
2016/03/06

Outline

- Technological goals towards SKA
- Vivaldi concept
- Design for cost
- Design for power



Design team ASTRON AAMID frontend workpackage

▪ Michel Arts	Antenna researcher
▪ David Prinsloo	Antenna engineer
▪ Robert van den Horn	Mechanical engineer
▪ Raymond van den Brink	Industrial engineer
▪ Erik van der Wal	RF system specialist
▪ Martijn Brethouwer	RF designer
▪ Lesley Goudbeek	RF designer / photonics
▪ Albert van der Duin	Microcontroller engineer
▪ Sieds Damstra	Hardware/Software engineer

Funding secure for 2016 - 2018

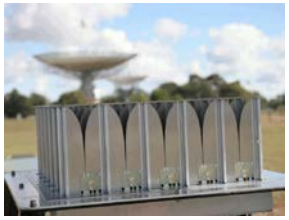
Technological goals towards 2025

- TRL level
- Performance improvement

- Total cost
- Total Power

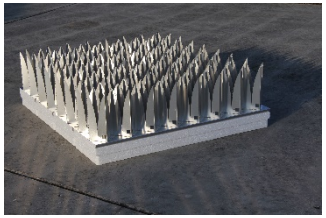
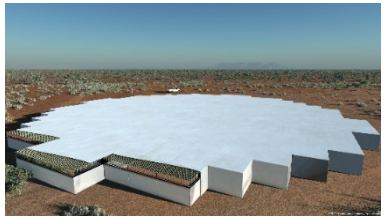
Towards SKA 2025





Dwingeloo (NL) : 28m²
Karoo (SA) : 4m²
UCT, Stellenbosch, Others? : 4m²

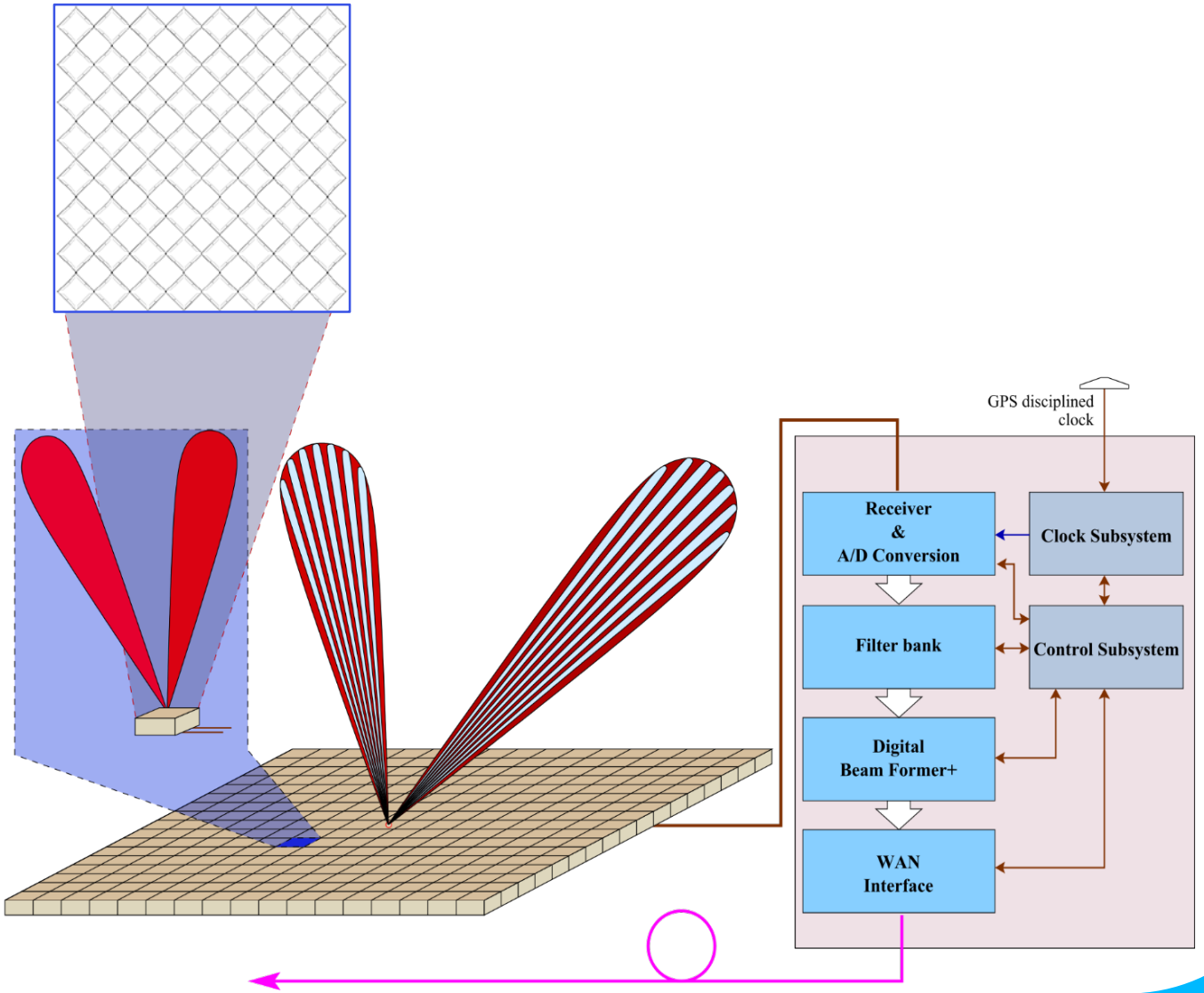
2016 2018 2020 2022 2024 2026

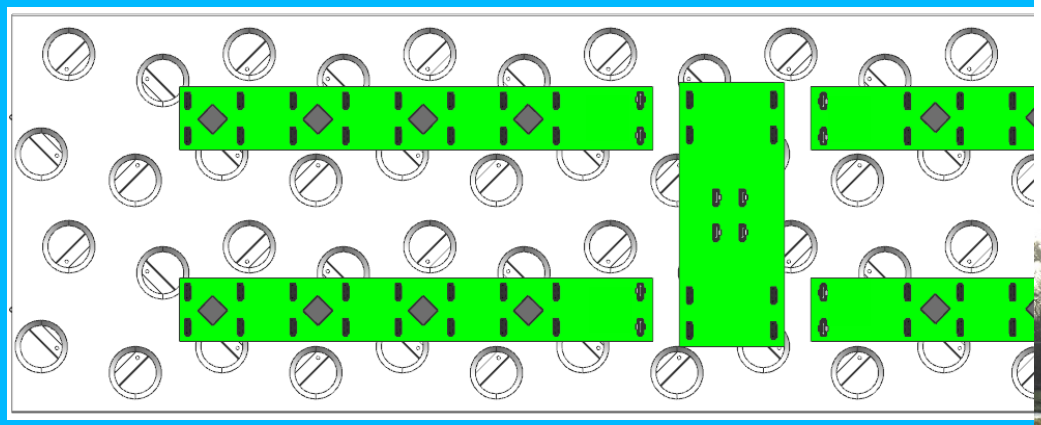

Tile requirements (Working assumptions)

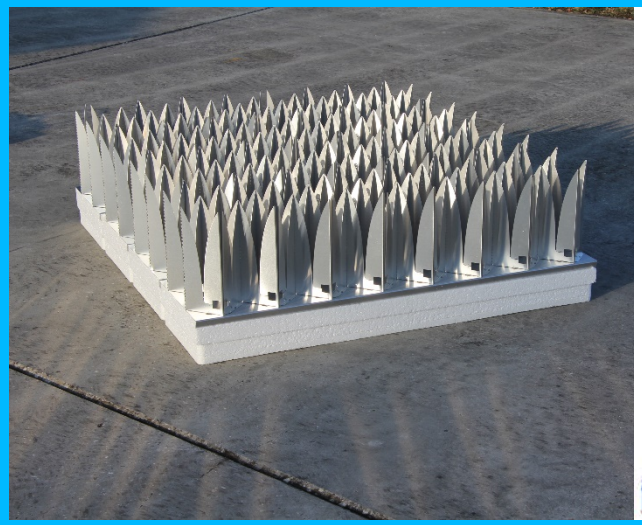
Requirement	Requirement	Unit
Frequency Range	450 - 1450	MHz
Optical FOV	> 100	Sq. Deg
Area	2000	M^2
Flagged data during observation	< 5	%
T receiver	40 (2016)	K (30K in 2025)
Instantaneous RF bandwidth	500	MHz
Power	50	W/M^2 Goal 2025
Cost	1000	€ Goal 2025
Polarization	2	Full stokes
Analog Beams	2	Per tile

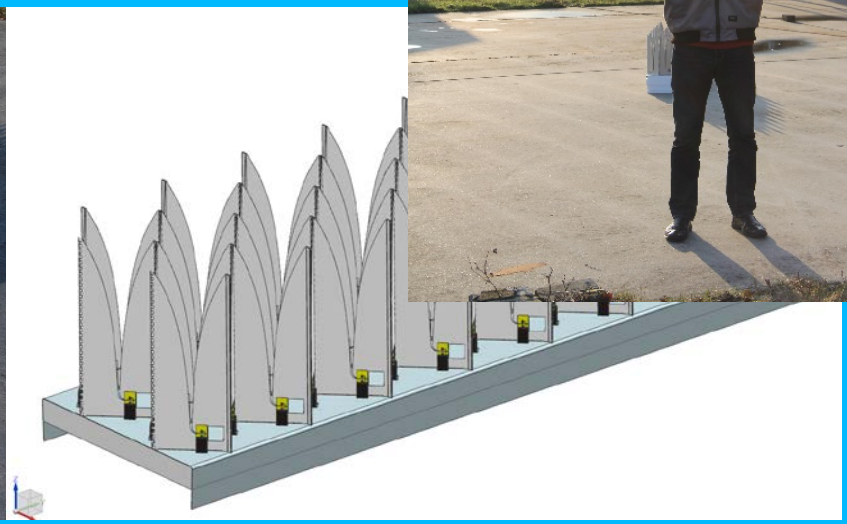
A station


GPS disciplined clock
Receiver & A/D Conversion
Clock Subsystem
Filter bank
Control Subsystem
Digital Beam Former+
WAN Interface

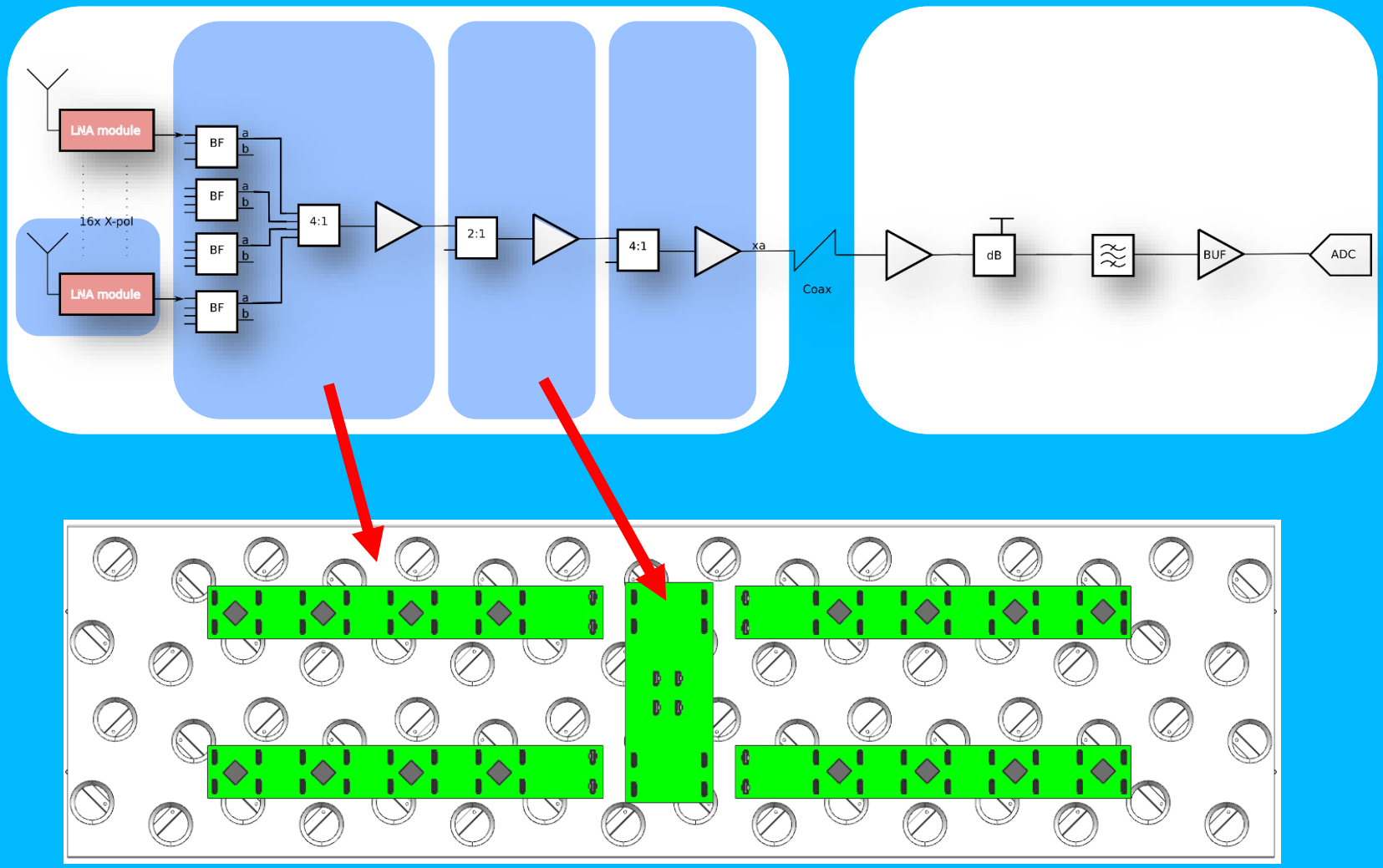
AAMID – 2016 prototype







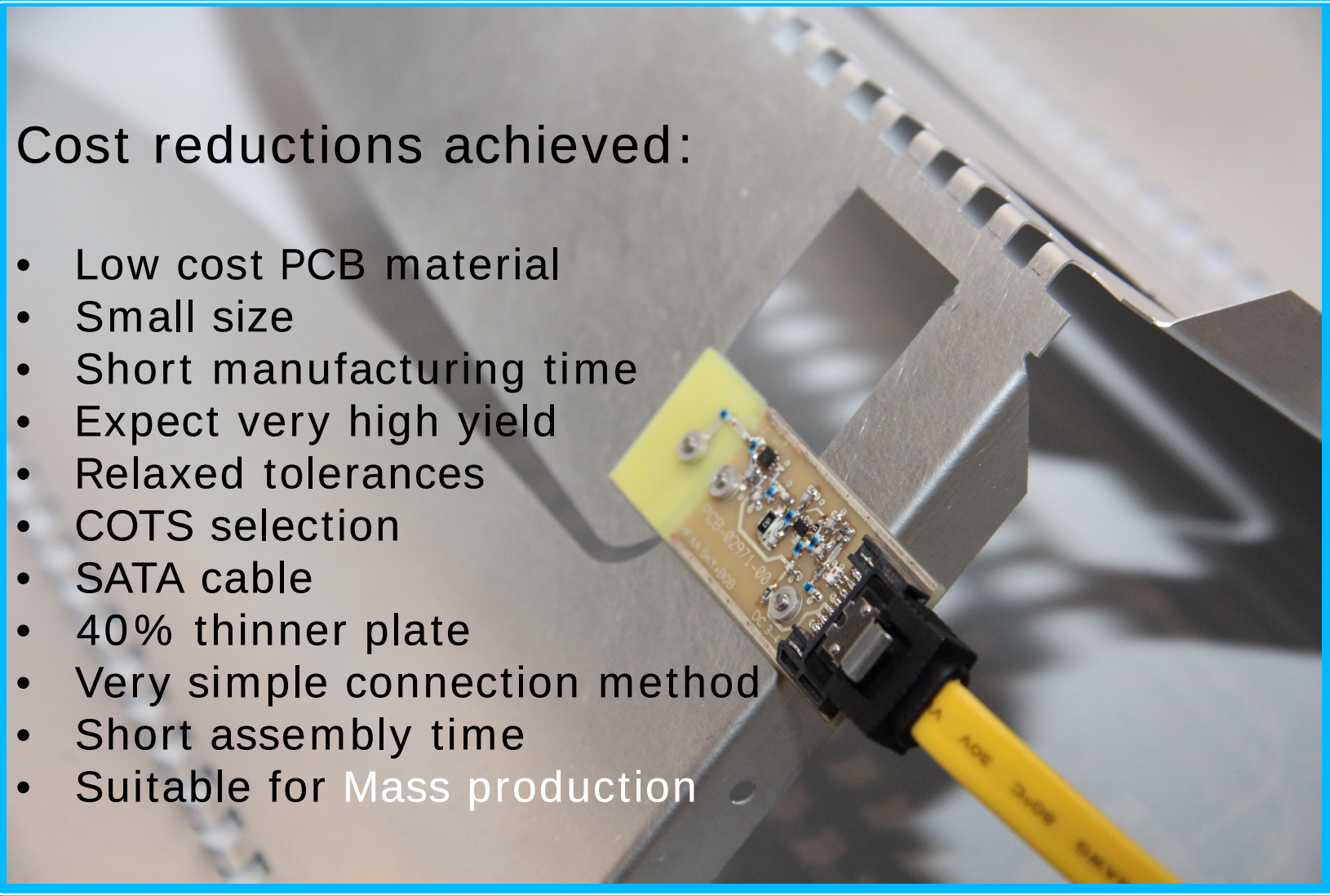
RF block diagram (for 1 pol., 1 beam)



Design for Manufacturing towards SKA

- Keep it simple!
- Design for the complete system
- Take complete lifecycle into account from cradle to the grave
- Due to the large numbers;
  every penny/cent counts
- Buy parts / Components of the shelf (COTS)
- Design For Manufacture and Assembly
- NRE is divided by the millions of elements

Example; LNA module & Antenna



Cost reductions achieved:

- Low cost PCB material
- Small size
- Short manufacturing time
- Expect very high yield
- Relaxed tolerances
- COTS selection
- SATA cable
- 40% thinner plate
- Very simple connection method
- Short assembly time
- Suitable for Mass production

Cost assumptions

- EMBRACE is backed up by quotes
- Current concept 2016 is backed up by quotes
- High cost components estimated from EMBRACE / APERTIF volumes

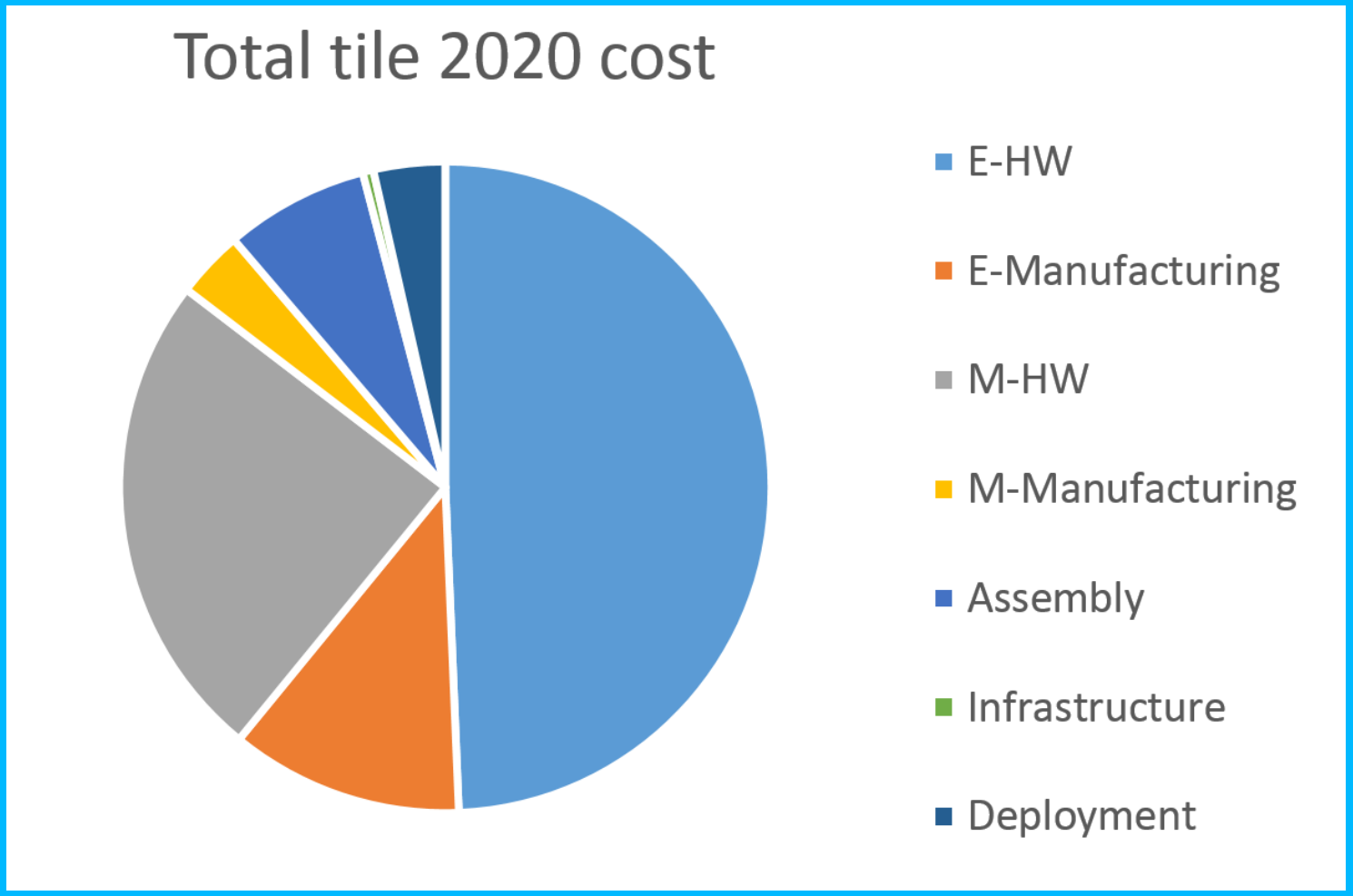
  Higher volume ==> cheaper manufacturing process
  Machine cost of 200.000 euro divided by 45e6 = 0.45 cent/part
  Same holds for NRE

- Mechanics = material. cost/kg x weight + manufact. cost
- Electronics = comp. cost + 10 % manufact. Cost
- Profit margins not taken into account.

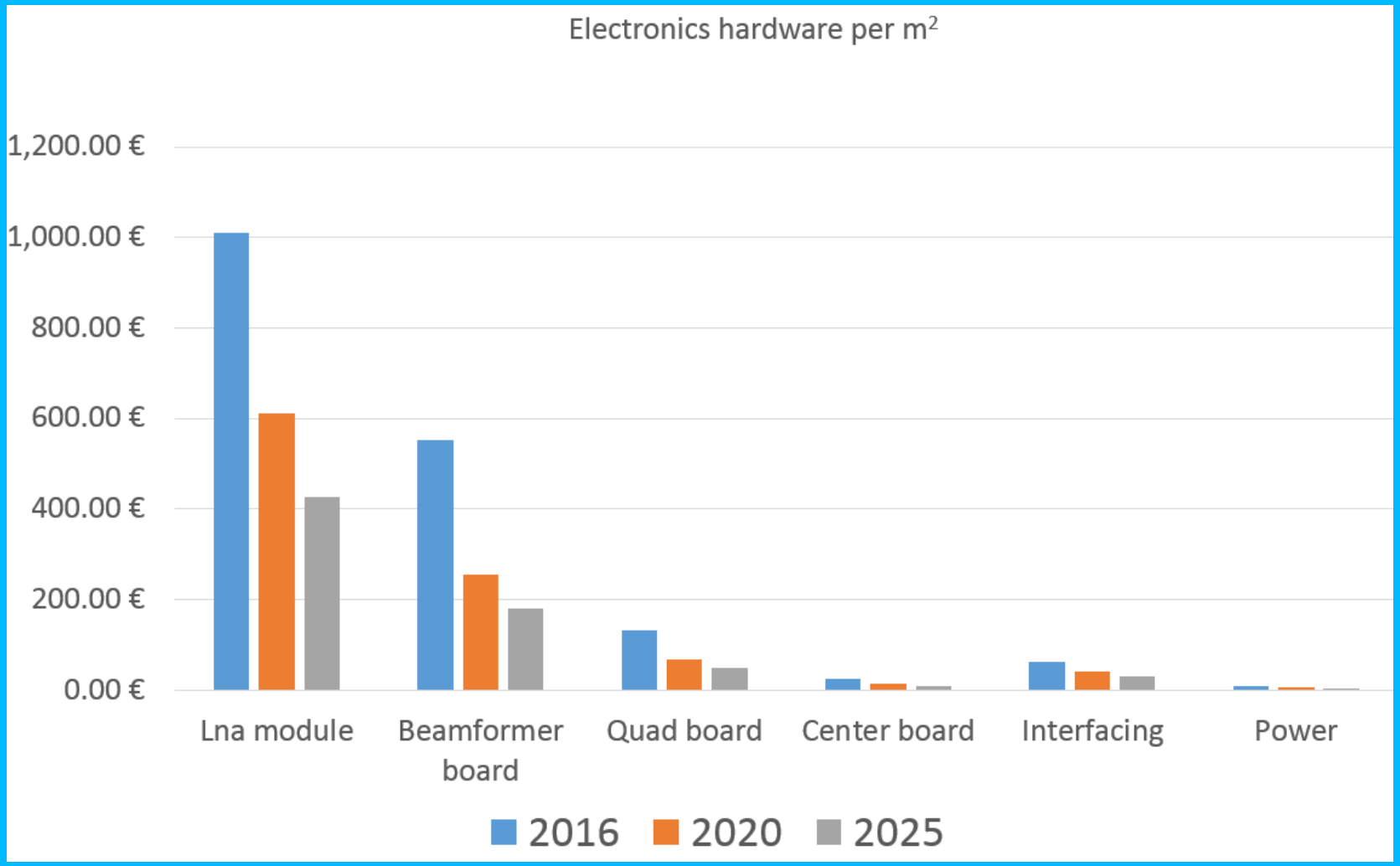
Cost areas:

- Mechanics = tile + frame + cover
- Electronics = PCB boards + components
- Infrastructure = cable infrastructure
- Deployment = Tile assembly + Testing + Ground Flattening

Total tile cost



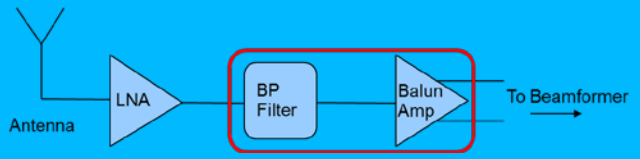
Electronic cost per square meter



Hardware – Electronics

Further cost reductions:

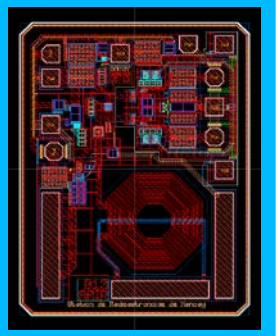
- IC integration
- Parts reduction
- Module size reduction
- 3D-MID
- Optimize manufacturing
- Thermode soldering

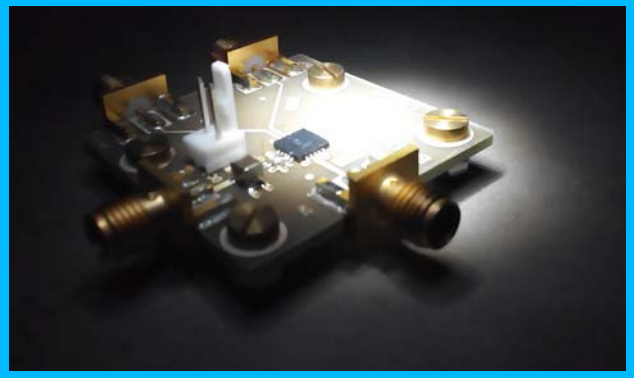


Station de Radioastronomie de Nançay
AAIR project

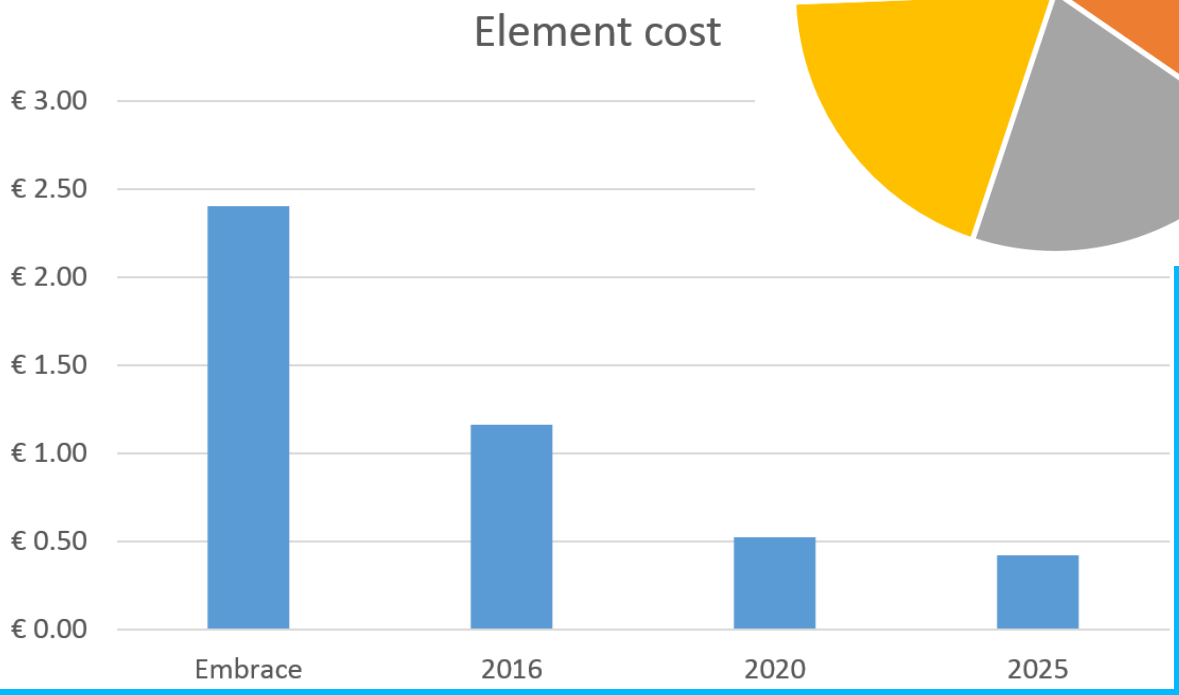
Surface = 1.142 mm2
NXP QuBiC4Xi Technology

Asics in QFN Package
HVQFN20_SOT662BB3

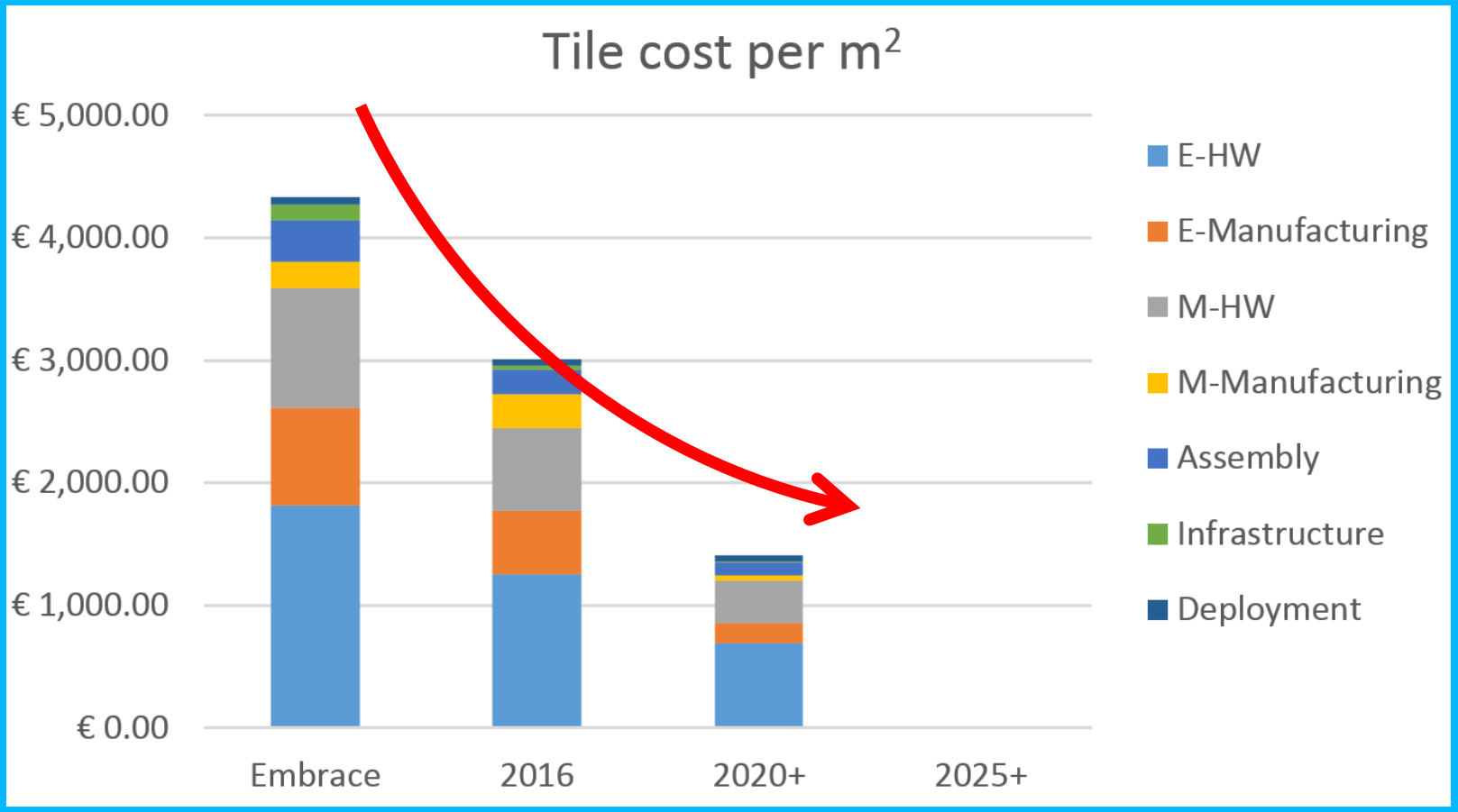




Hardware - Mechanics



Cost towards SKA 2025

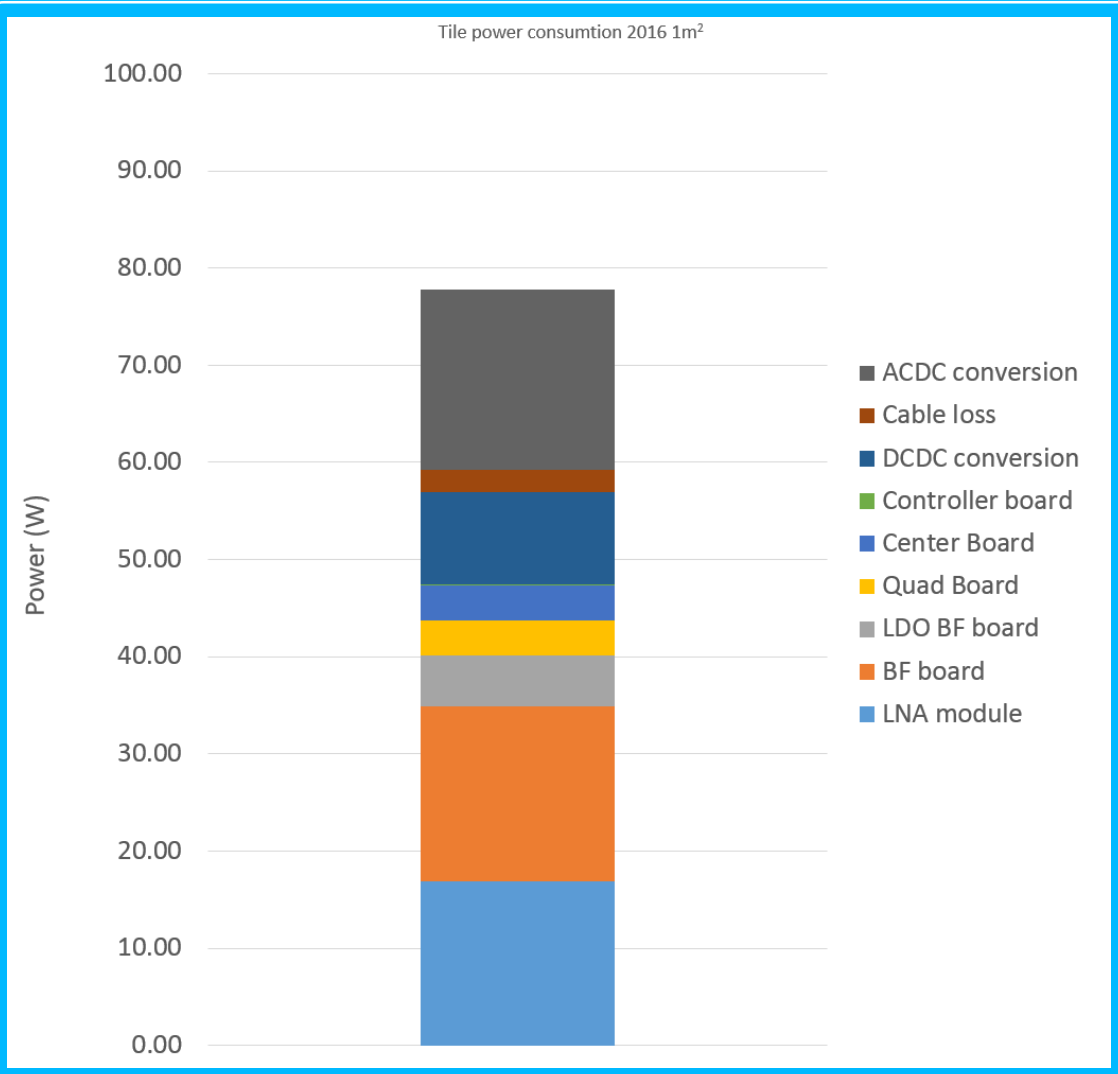


Electronic HW cost confirmed by manufacturers

Power assumptions

Nr of elements per m2	128	2 pols
LNA module	132	mW
BF board	627	mW
Quad Board	452	mW
Center Board	212	mW
Power conversion efficiency	80	%

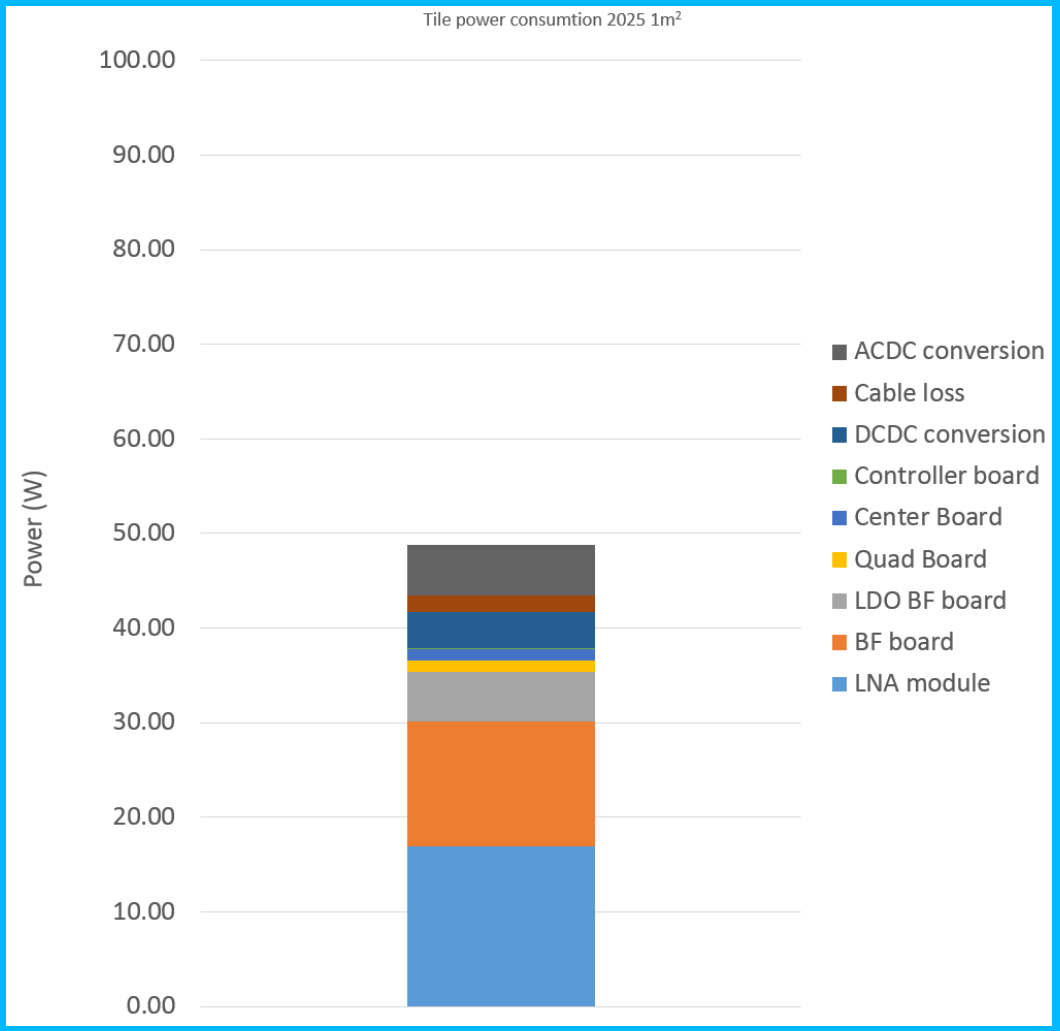
Tile power consumption W/m^2
2016 tile



Power reductions:

- Relax of linearity requirements due to better RFI situation
- Amplifier technology change
- Efficient power conversion scheme
- Minimize losses

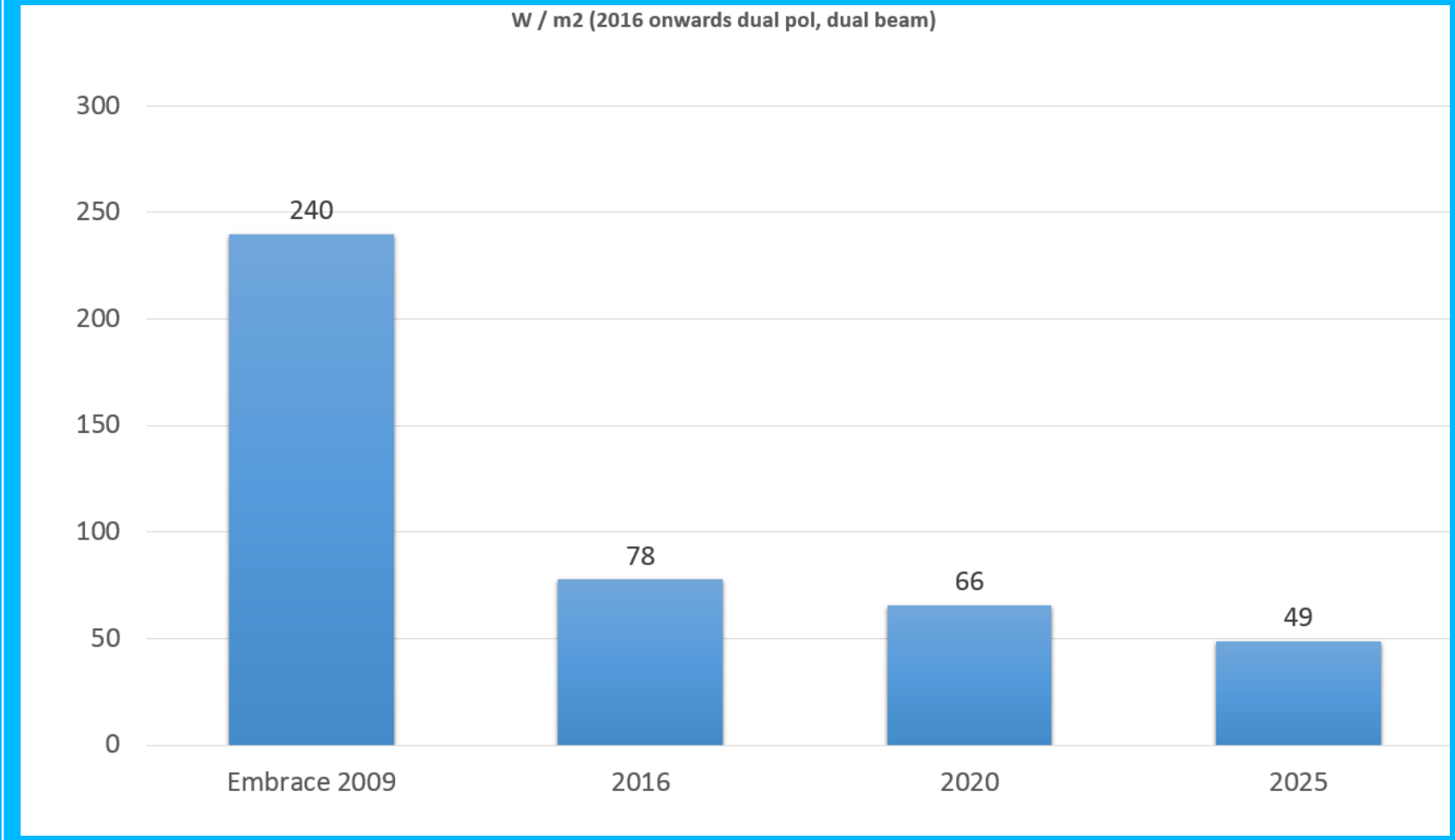
Tile power consumption W/m^2
2025 tile



Road to 2025:

- Improve concept
  - The <u>right</u> Technology selection
  - Balance power / performance
- Reduce power conversion losses

AAMID tile power consumption (Watt / m²)



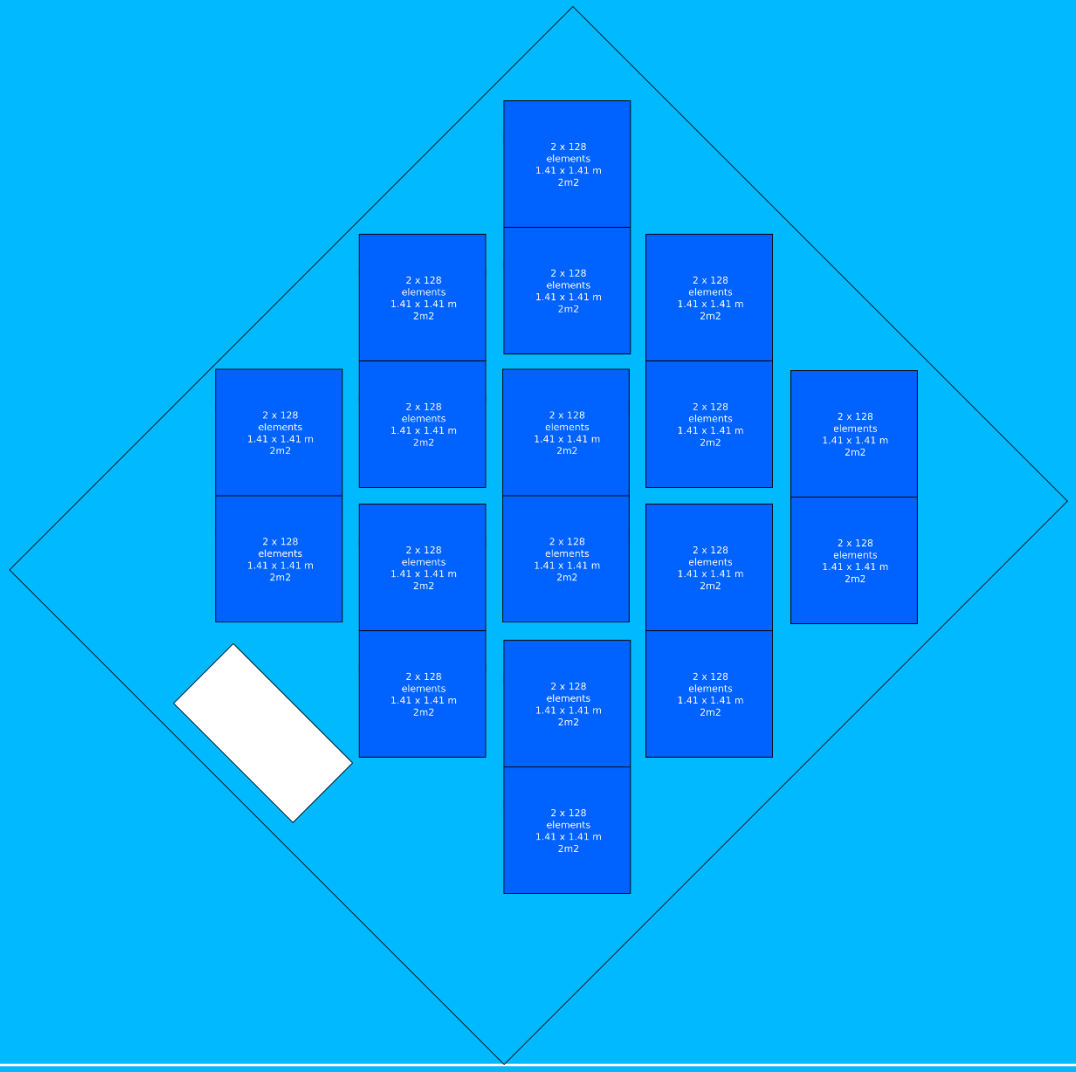
Summary

Working with great team to achieve our goals:

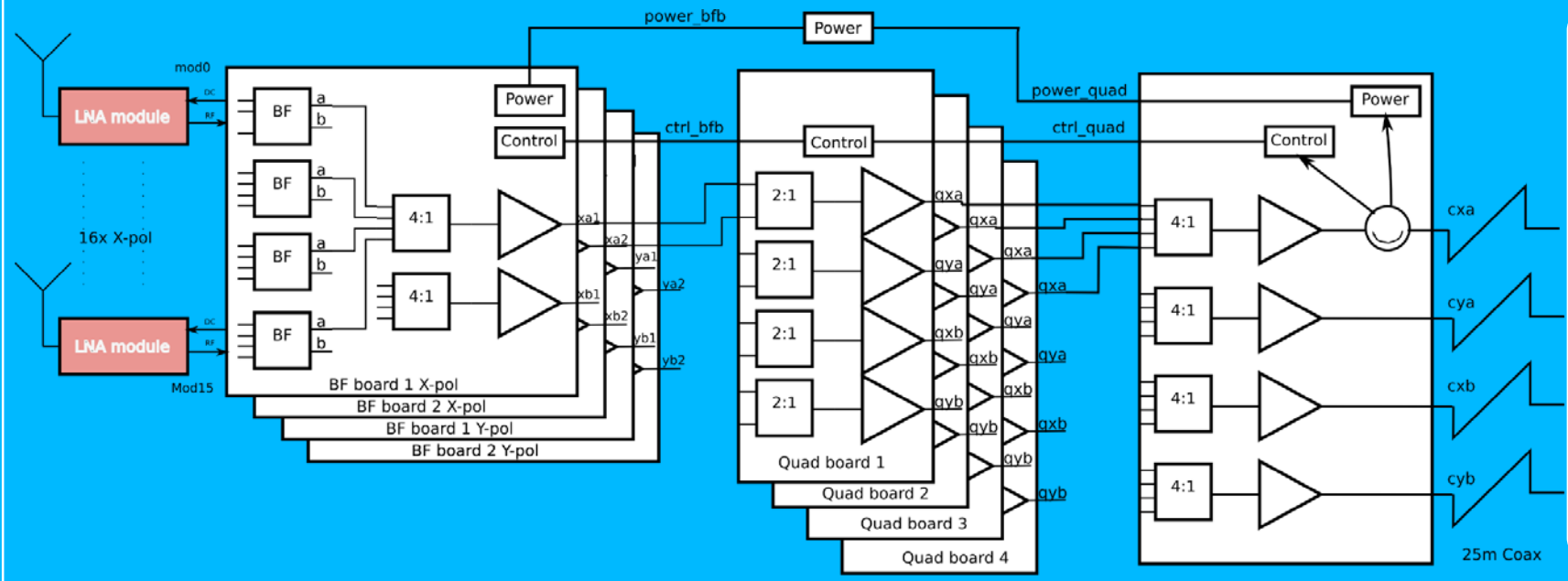
- Performance increase over frequency and scanangle
- TRL level increase by demonstrating working tiles in the Karoo
- On track for 1000 euro per square meter goal.
- Power consumption of 50W per square meter is feasible!

<u>We can do this, and make discoveries happen!</u>

28m2 array



RF tile block diagram (versimpelen) + boards to be build



Tile to backend