Receivers for Dish and WBSPF

Stéphane GAUFFRE
WBSPF
SKA AIP Meeting
Dwingeloo, Friday 9 June 2017

Outline

- Receiver overview
- Part on Indexer
  - RF Chains
  - Digitizer Board
  - Data Transmission
  - Clock Conditionner Module
- Part in Pedestal
  - Data Reception
  - FPGA Carrier Board

Receiver Overview

WIDE BAND SINGLE PIXEL FEEDS

- Requirements:
  - SPFRx input return loss > 15 dB
  - SPFRx input protection: no damage for an input signal of +10 dBm
  - SPFRx gain flatness: 1.5 dBp-p (TBC)
  - SPFRx nominal input signal: -132 dBm/Hz to -12 dBFS
  - SPFRx noise figure < 25 dB
  - SPFRx attenuation range: 0 – 40dB for Band 4 and 0 – 37dB for Band 5

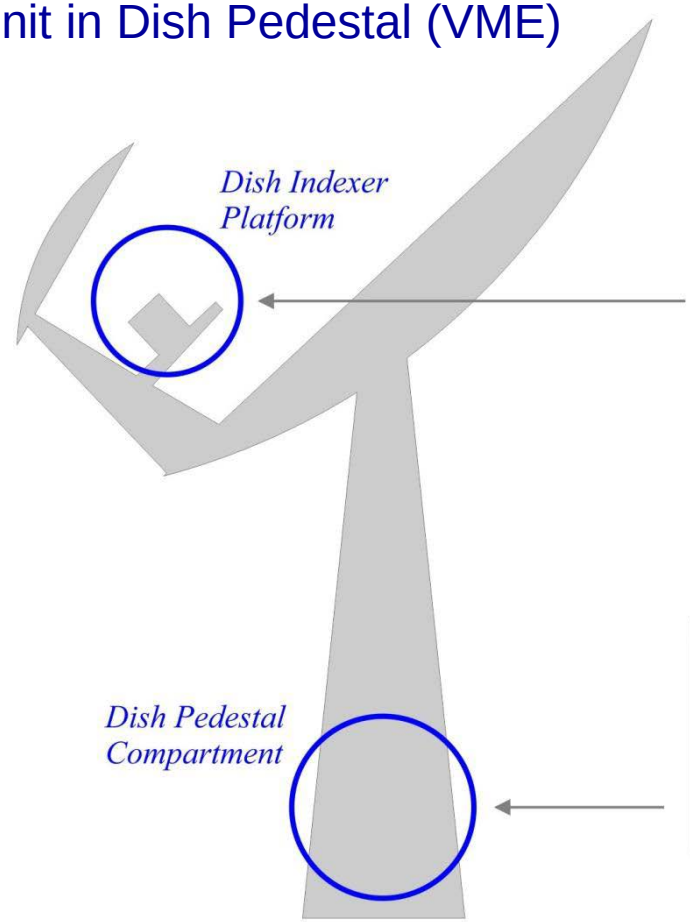
	Freq. Range	BW	Min bit depth	Transport
Band 4	2.8 – 5.18 GHz	2.38 GHz	4	2 × 4 × 6 GSps
Band 5a	4.6 – 8.5 GHz 5.0 – 9.25 GHz ***	3.9 GHz 4.25 GHz	3	2 × 4 × 2 × 6 GSps
Band 5b	8.3 – 15.3 GHz 9.0 – 16.7 GHz ***	7.0 GHz 7.7 GHz	3	2 × 4 × 2 × 6 GSps
Band 5c	15 – 24 GHz 16.5 – 24 GHz ***	9 GHz 7.5 GHz	3	2 × 4 × 2 × 6 GSps

*** Band 5 ECP160022 ECP approved

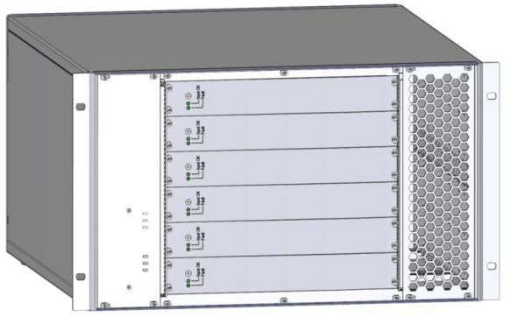
Receiver Overview

WIDE BAND SINGLE PIXEL FEEDS

- Receiver on Dish indexer
- Data transport over optic fiber
- Digital processor unit in Dish Pedestal (VME)



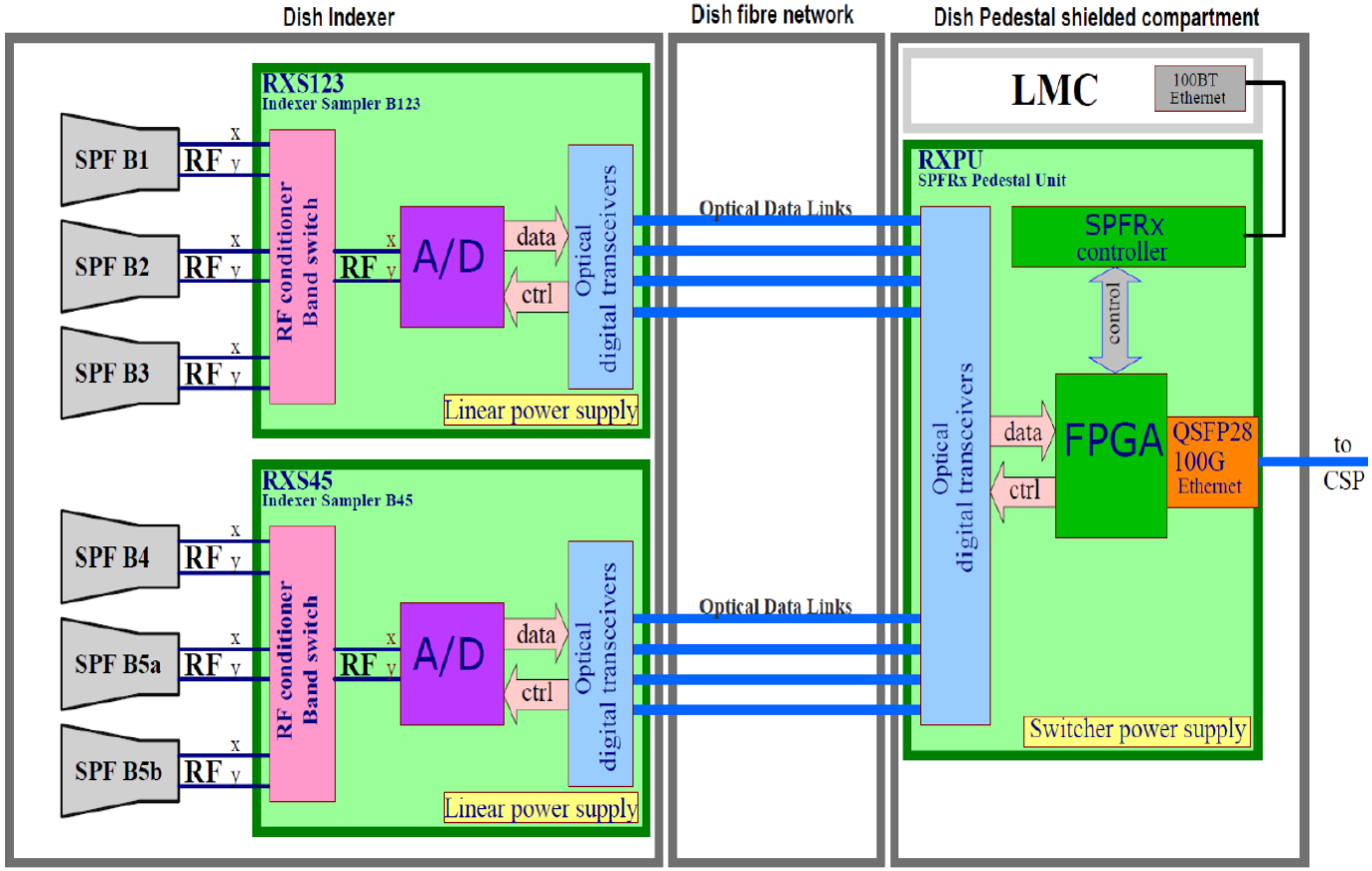
SPFRx Indexer Sampler



SPFRx Pedestal Unit

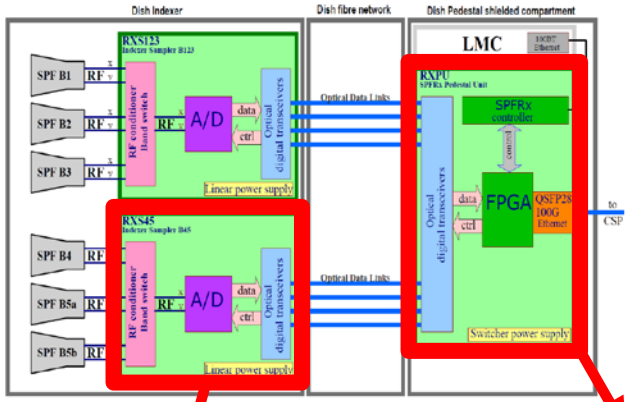
Receiver Overview

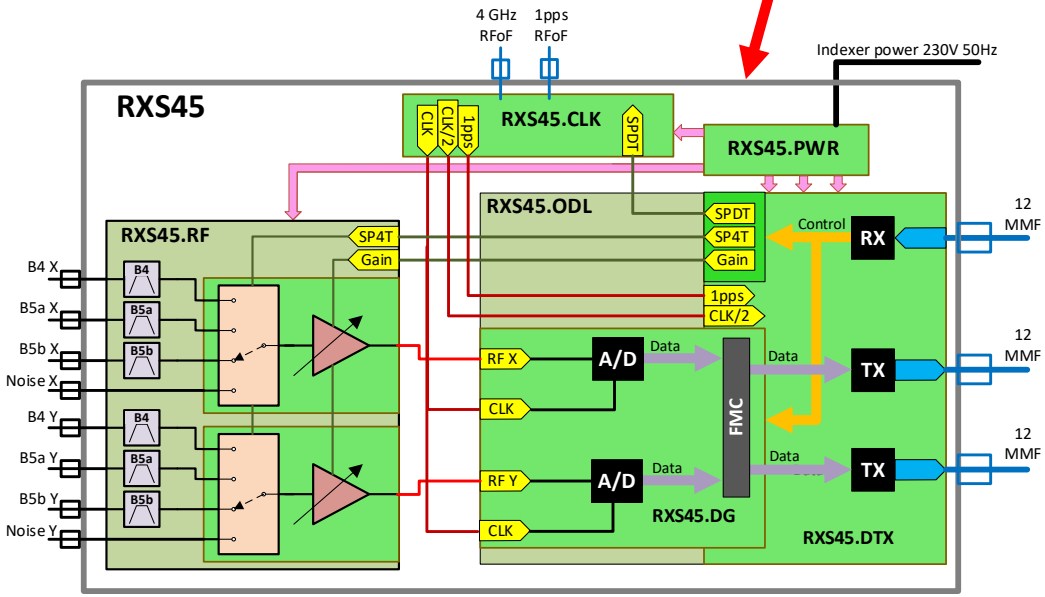
- Receiver on Dish indexer
- Data transport over optic fiber
- Digital processor unit in Dish Pedestal (VME)

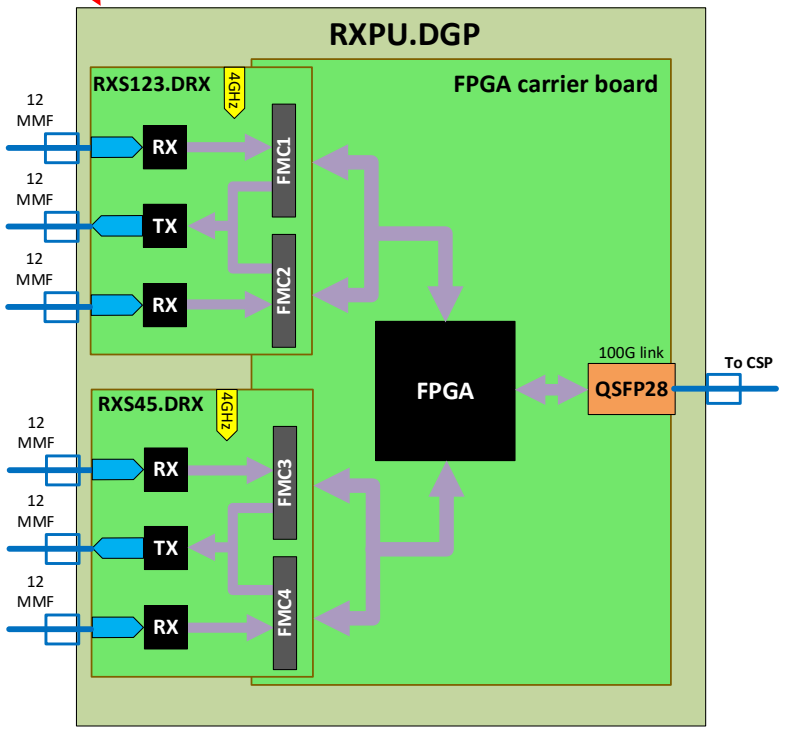


Receiver Overview

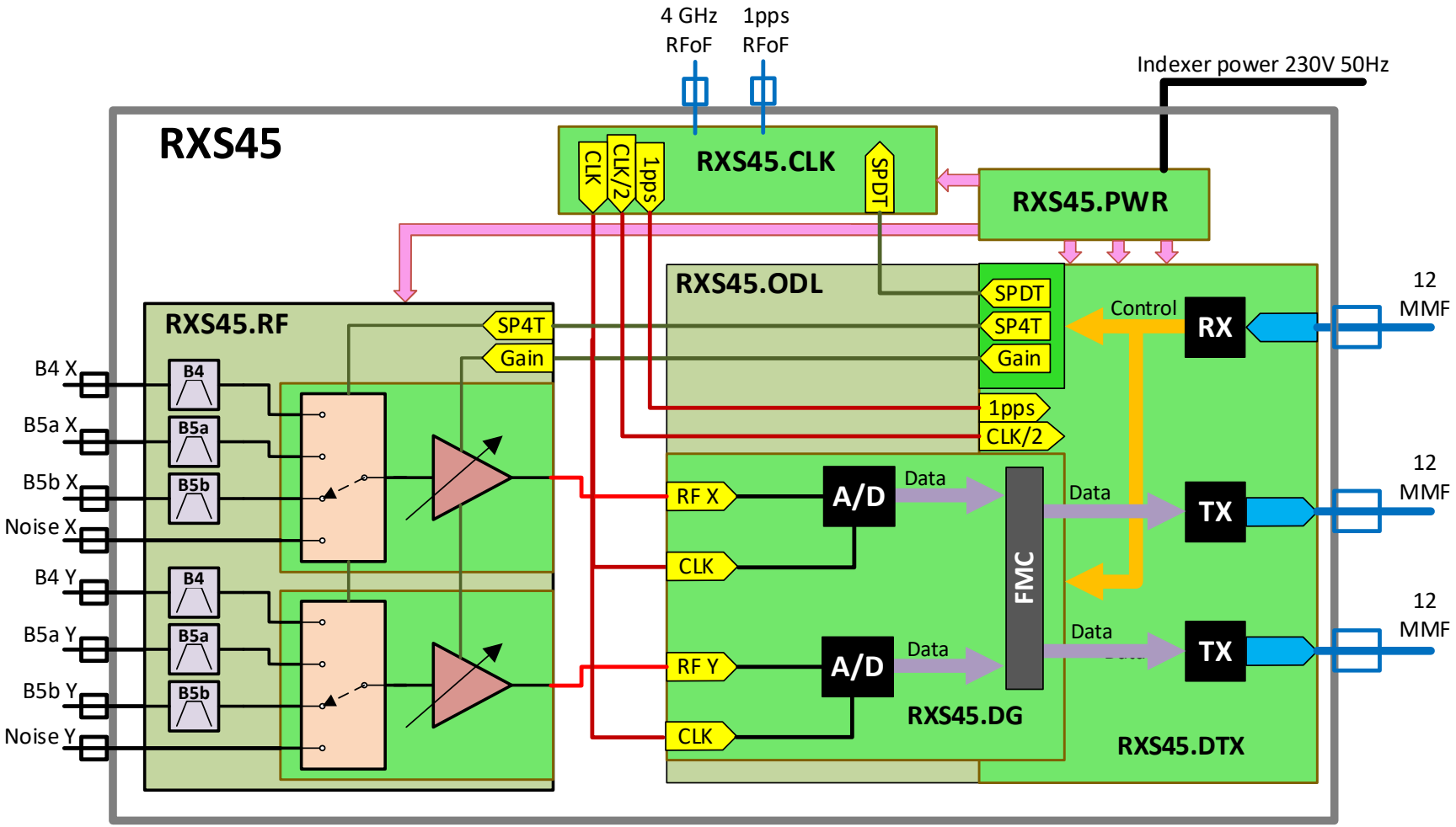
WIDE BAND SINGLE PIXEL FEEDS







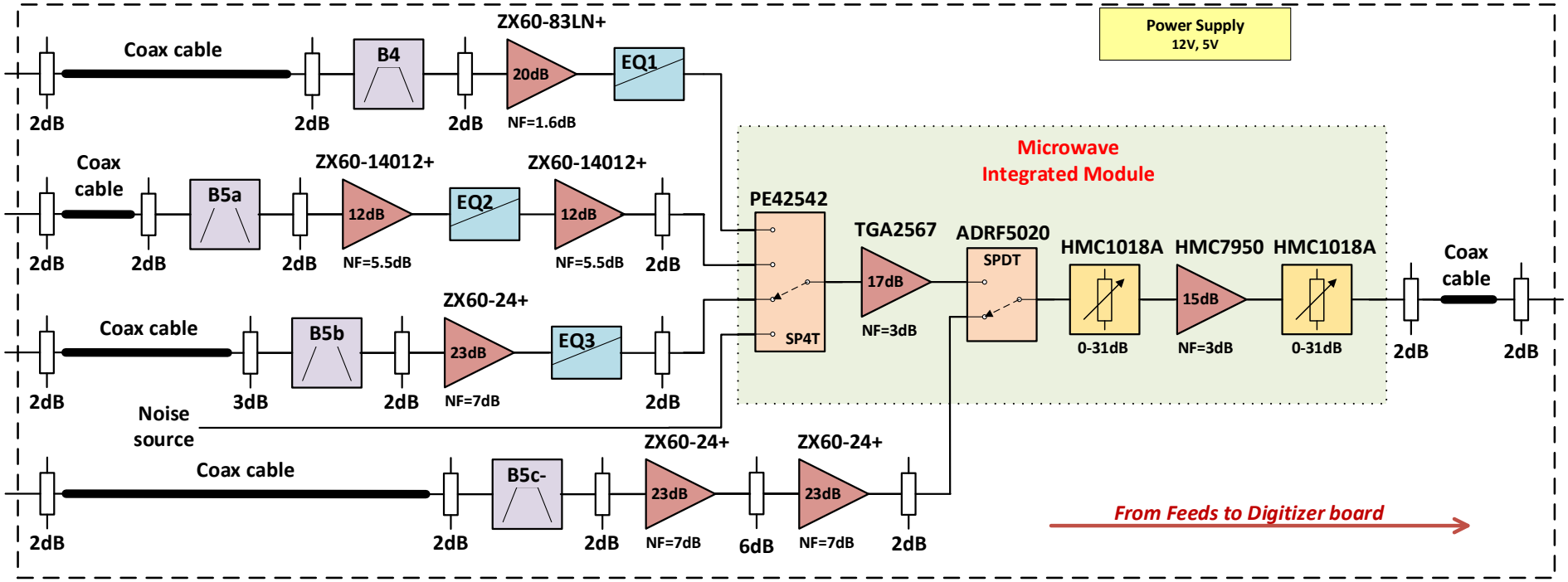
Part on feed indexer



RF Chains: RXS45.RF

WIDE BAND SINGLE PIXEL FEEDS

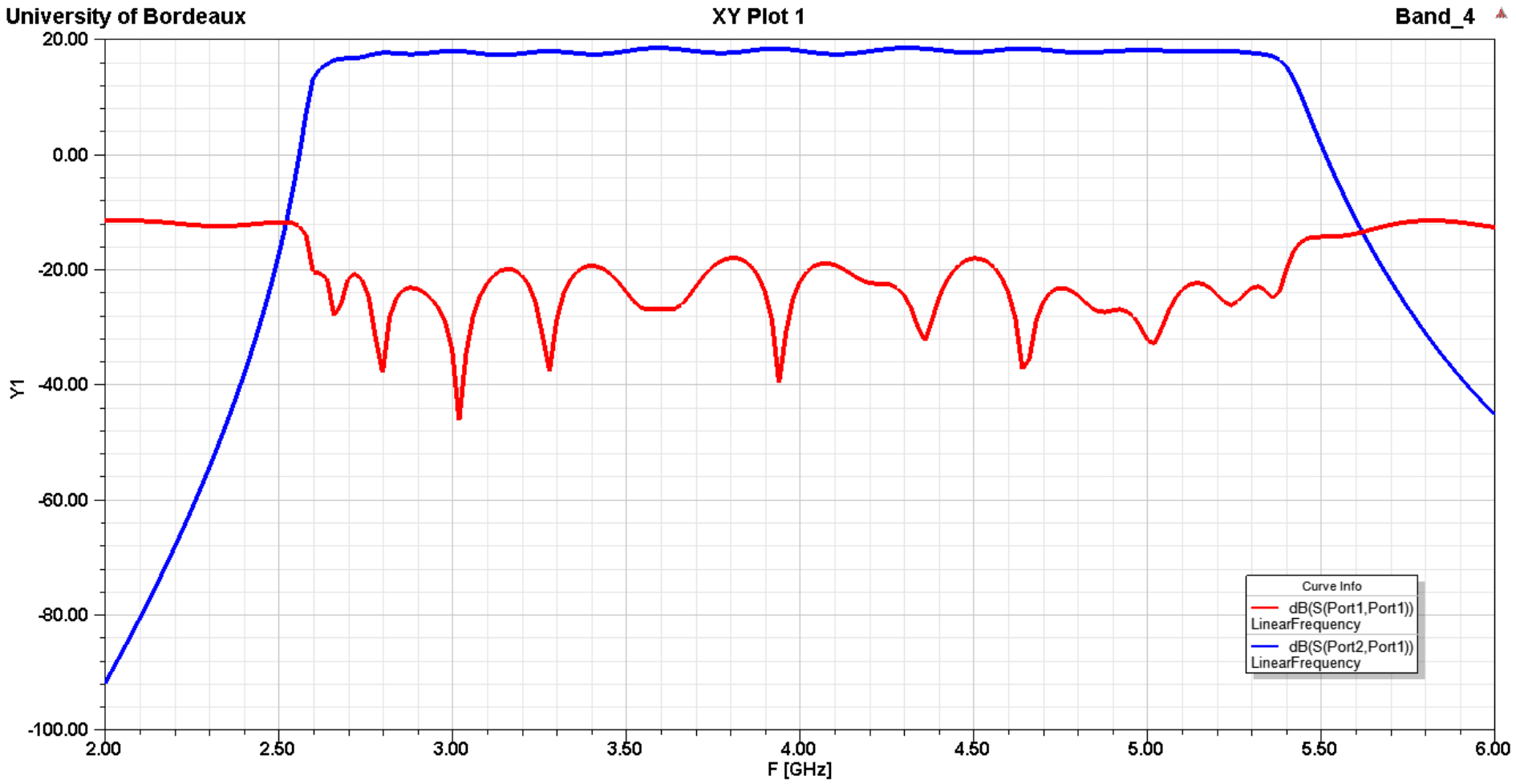
- Coaxial components: RF amplifiers (Mini-Circuits), gain equalizers (slope correction), SMA attenuators (input return loss, ripple)
- Custom band pass filters
- Surface mount devices for more integrated module (Cost and space saving)



RF Chains: Band 4 [2.8 – 5.18 GHz]

WIDE BAND SINGLE PIXEL FEEDS

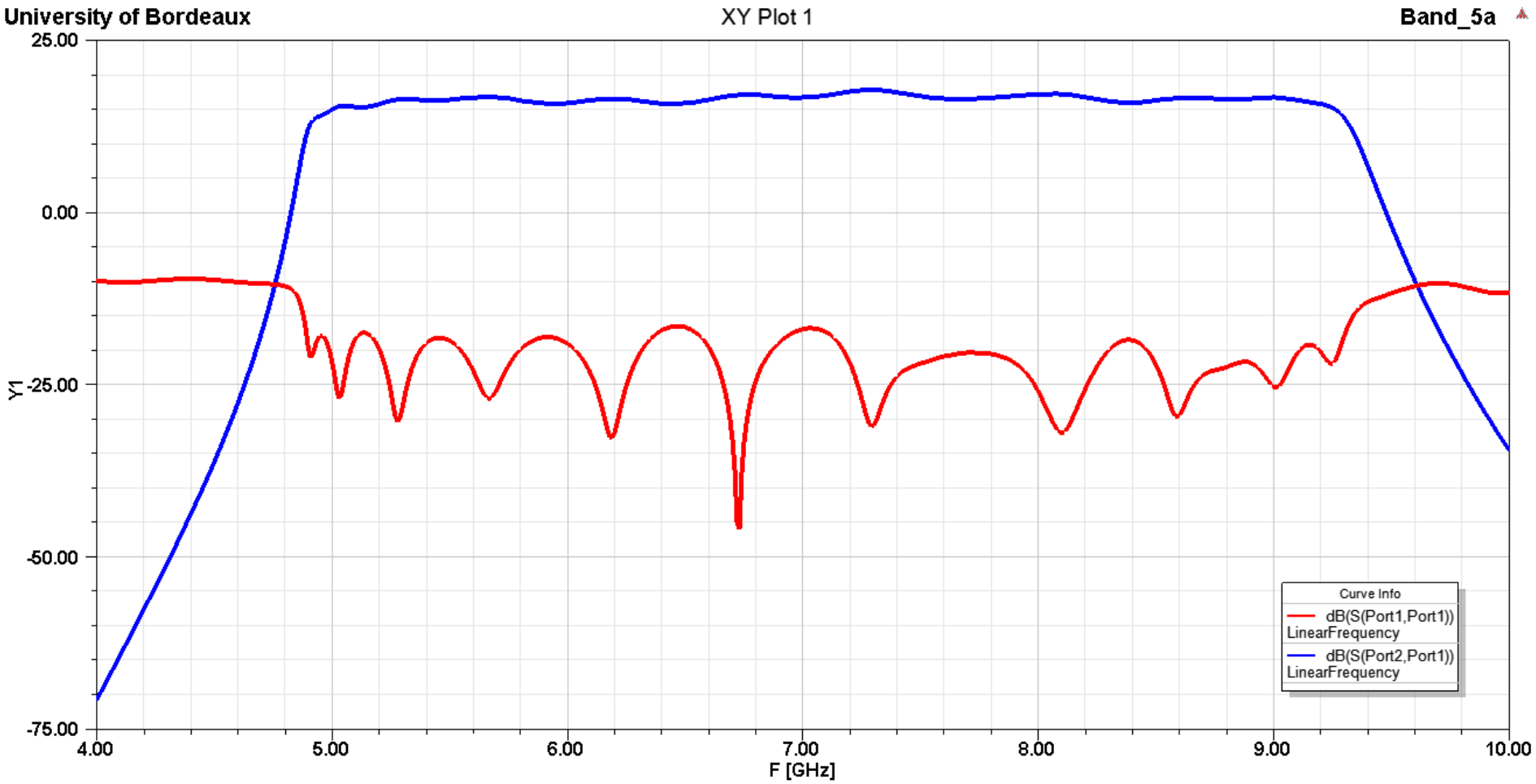
- Modeling with S-parameters



RF Chains: Band 5a [5 – 9.25 GHz]

WIDE BAND SINGLE PIXEL FEEDS

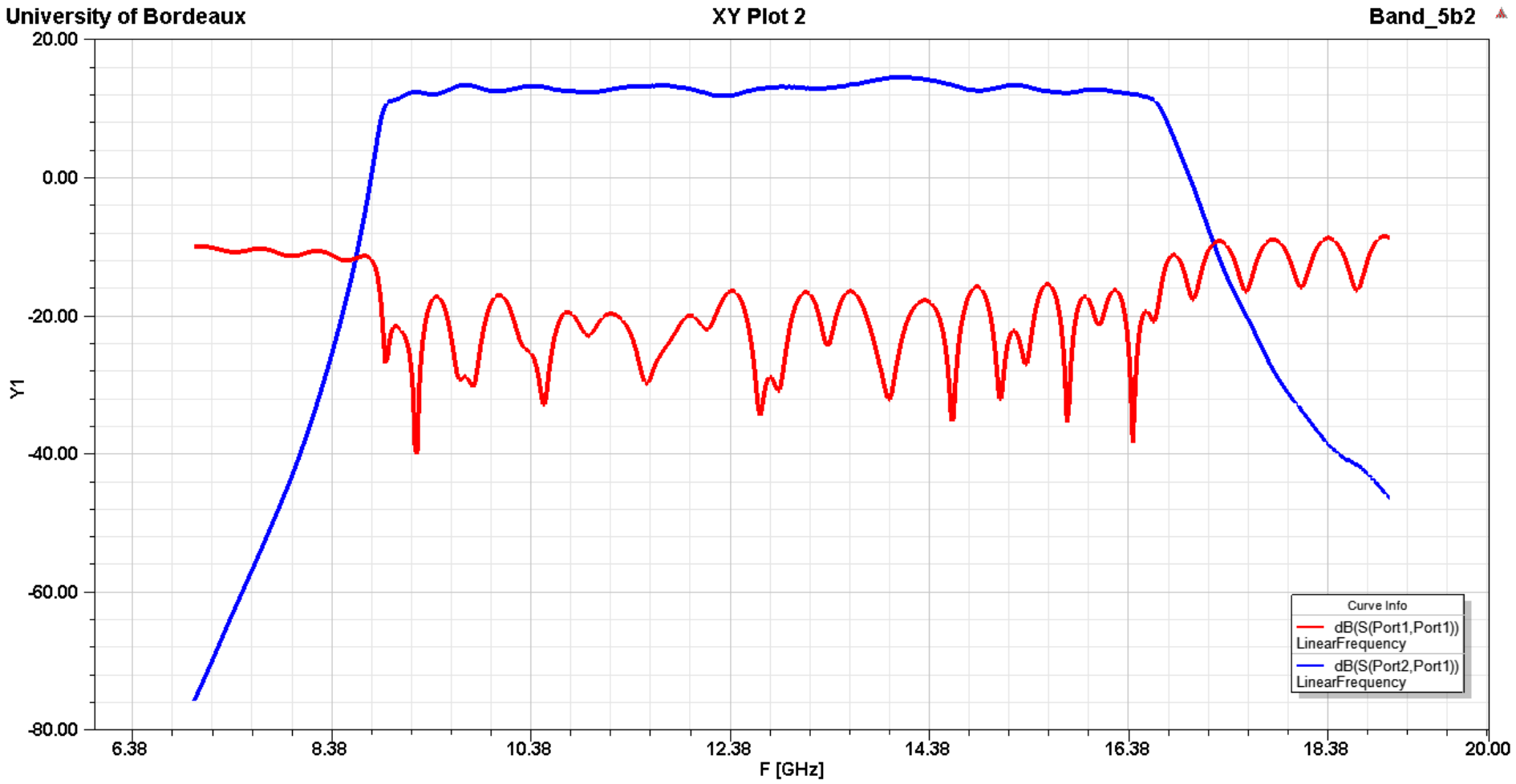
- Modeling with S-parameters



RF Chains: Band 5b [9 – 16.7 GHz]

WIDE BAND SINGLE PIXEL FEEDS

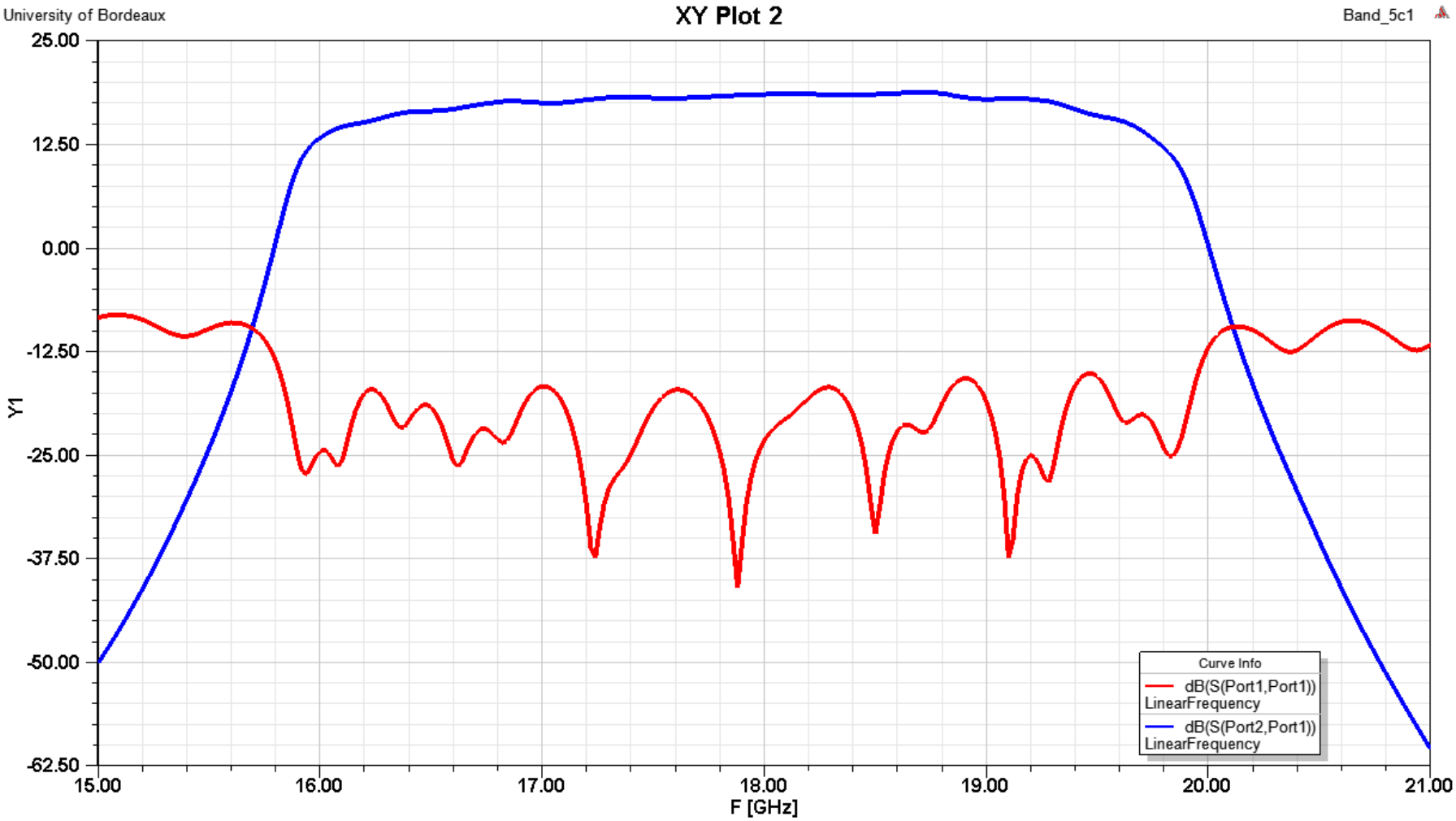
- Modeling with S-parameters



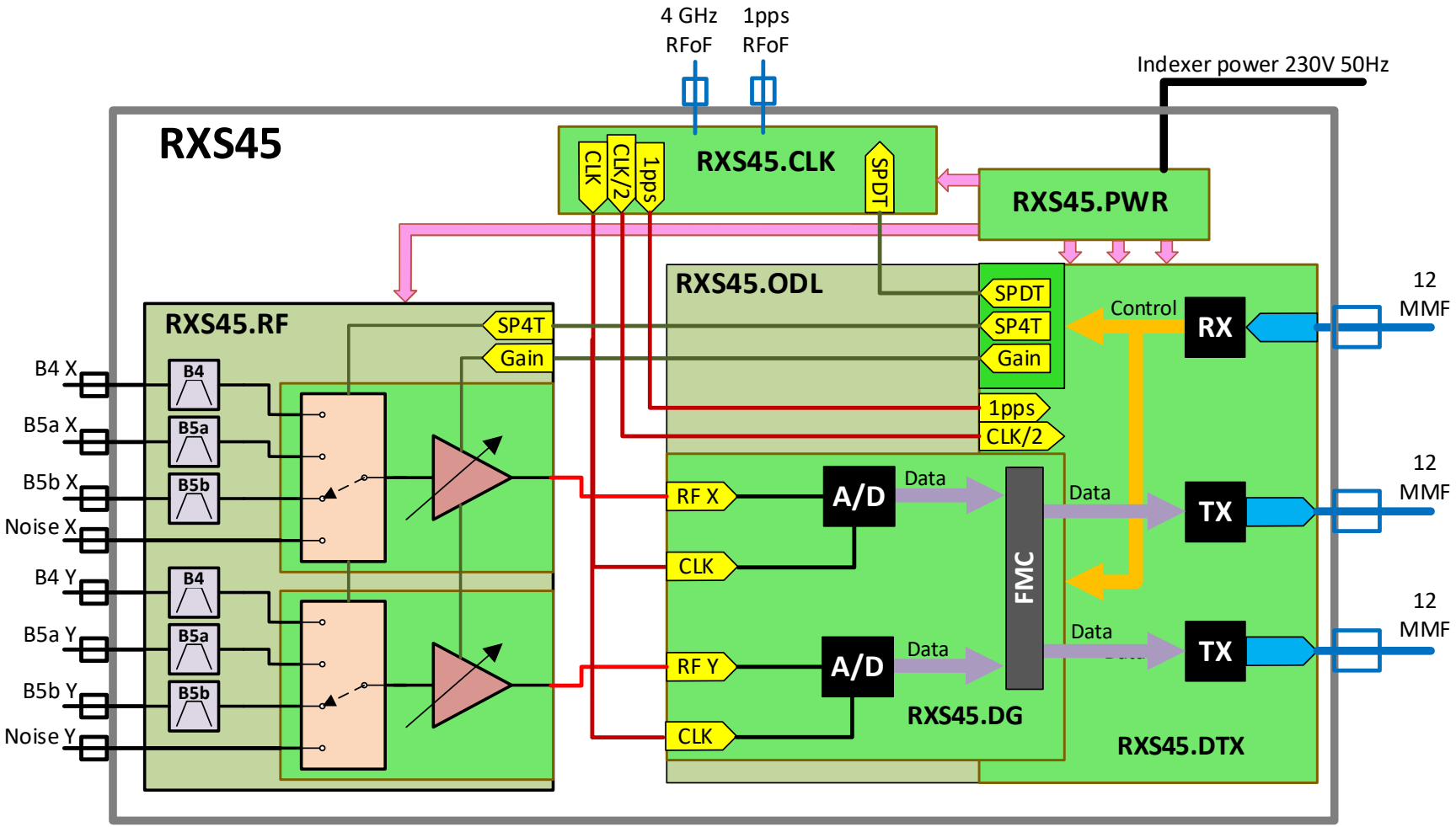
RF Chains: Band 5c [16.4 – 19.4 GHz]

WIDE BAND SINGLE PIXEL FEEDS

- Modeling with S-parameters



Receiver Part on Feed Indexer



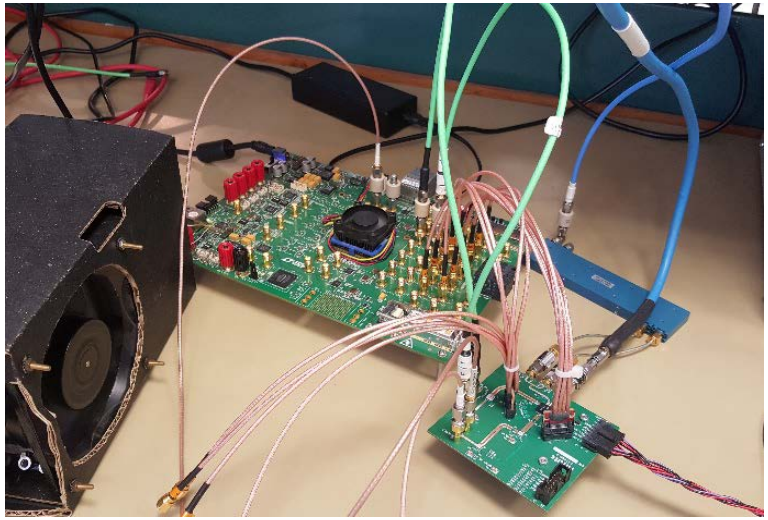
Digitizer Board: RXS45.DG

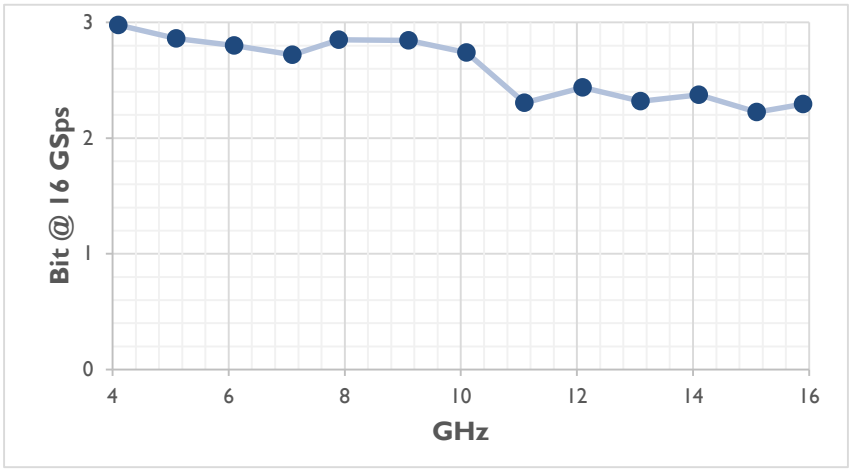
- COTS solution
- IP Macros are not considered (NRE cost > 1M€,)

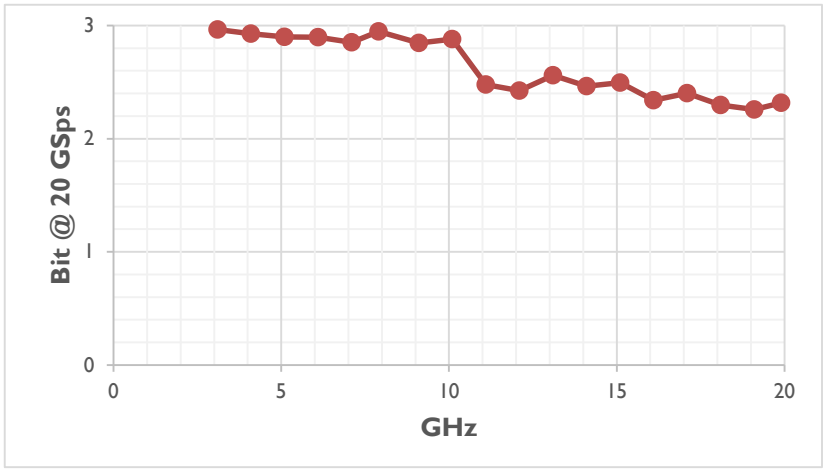
Parameter	ASNT7122 Adsantec	HMCAD5831 ADI	ADC2 Micram	A4B25G Alphacore
Input Bandwidth	**20 GHz**	**20 GHz**	25 GHz	25 GHz (TBC)
ENOB at 8GHz	3.23 at 10 GSps	**2.9 at 20 GSps**	5 at 20 GSps	3.3 at 25 GSps
Sampling (max)	**15 GSps**	26 GSps	32 GSps	25 GSps (TBC)
Power	**4.3 W**	**4.2 W**	**10 W**	0.5 W
Architecture	Single-core	Single-core	**2 interleaved**	Single-core
Package	CQFP	QFN	Module	**Chip-on-board**
Availability	Yes	Yes	Yes	**No**
Price	1450€	1100€	**3000€ (+100k€ of NRE)**	**2500€ for some units**

Digitizer Board: RXS45.DG

- HMCAD5831 evaluated: single tone analysis



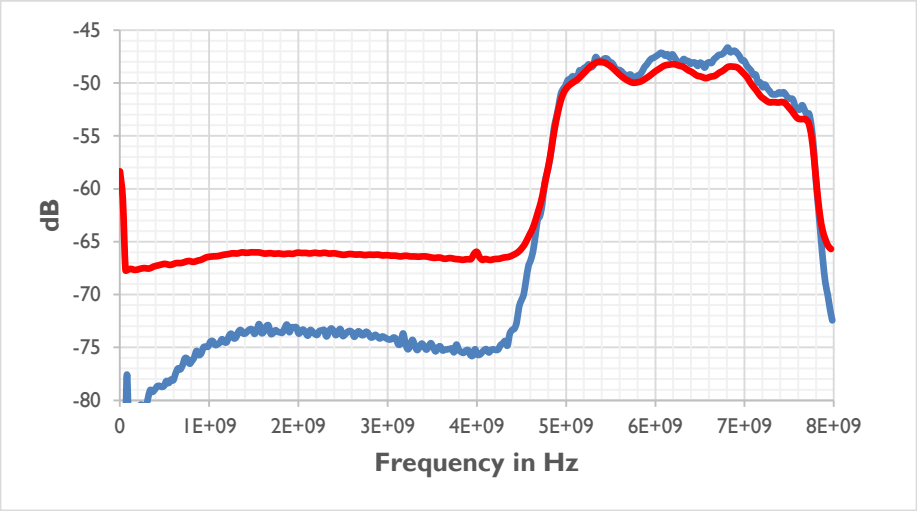




Digitizer Board: RXS45.DG

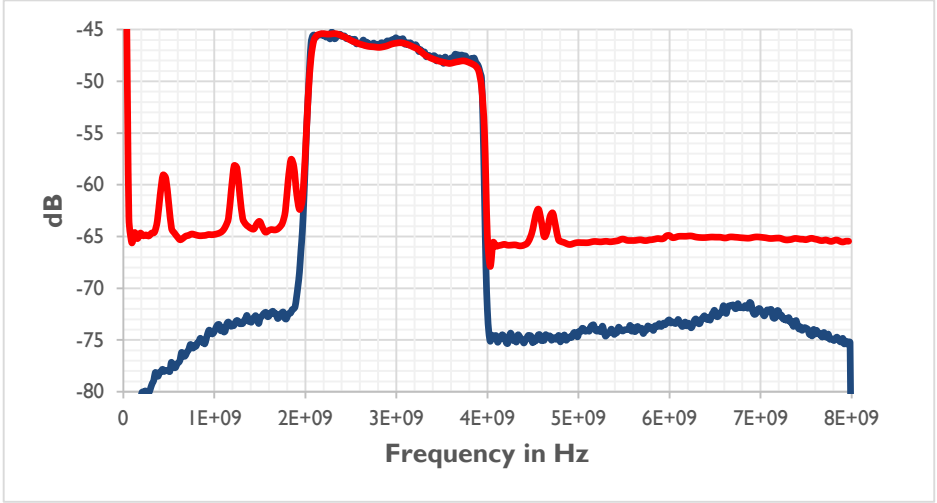
WIDE BAND SINGLE PIXEL FEEDS

- HMCAD5831 evaluated: noise analysis at 16 GSps



- 5 – 7.8 GHz Gaussain noise

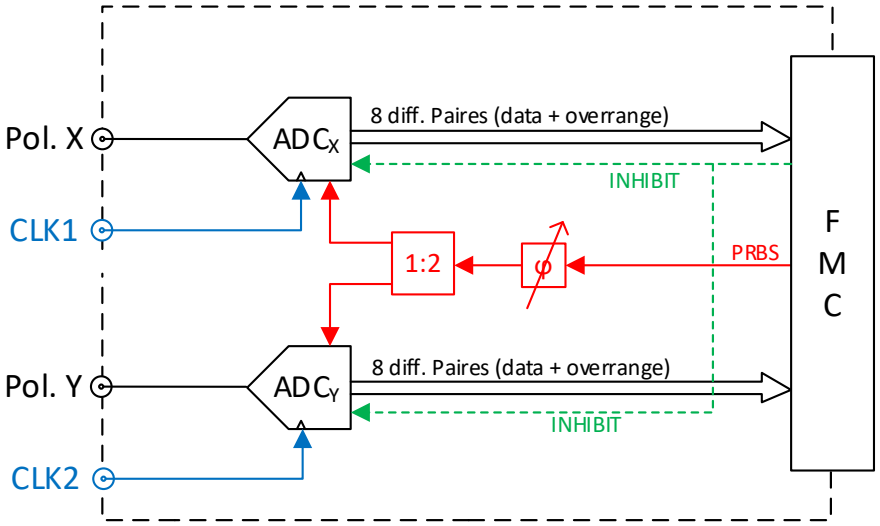
- 2.1 – 3.9 GHz Gaussain noise

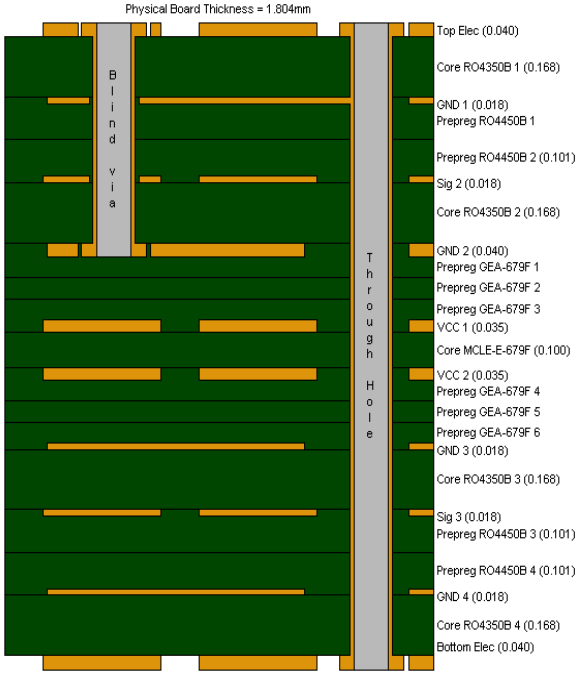


Digitizer Board: RXS45.DG

WIDE BAND SINGLE PIXEL FEEDS

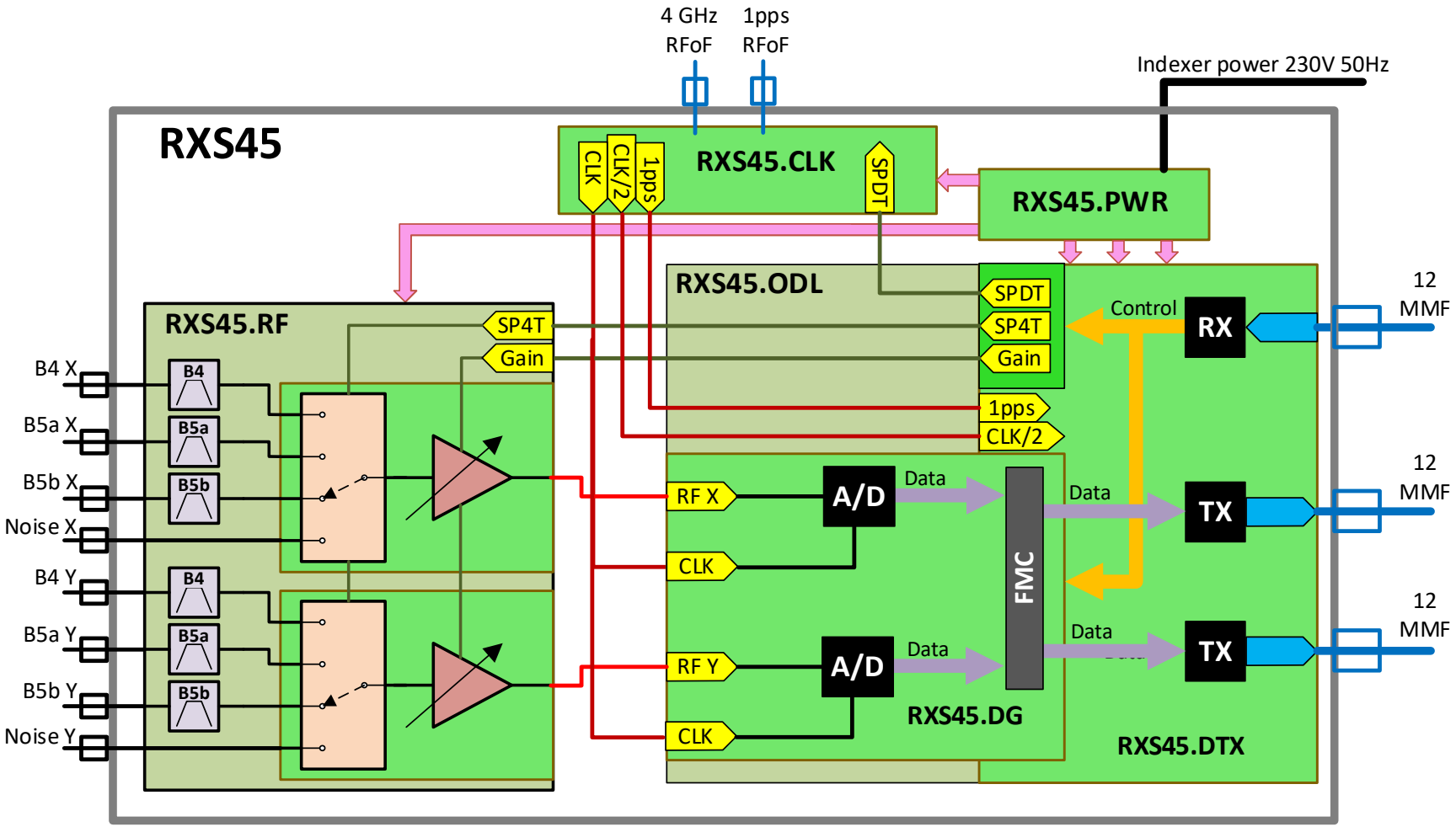
- First demonstrator based on the HMCAD5831





- Market survey:
  - Replace the HMCAD5831 board by a new one based on the Alphacore (4-bit at 25 GSps).
  - Discussion with E2V: 8-bit at more than 24 GSps in the E2V roadmap for space applications. Massive interleaved SAR architecture.

Receiver Part on Feed Indexer

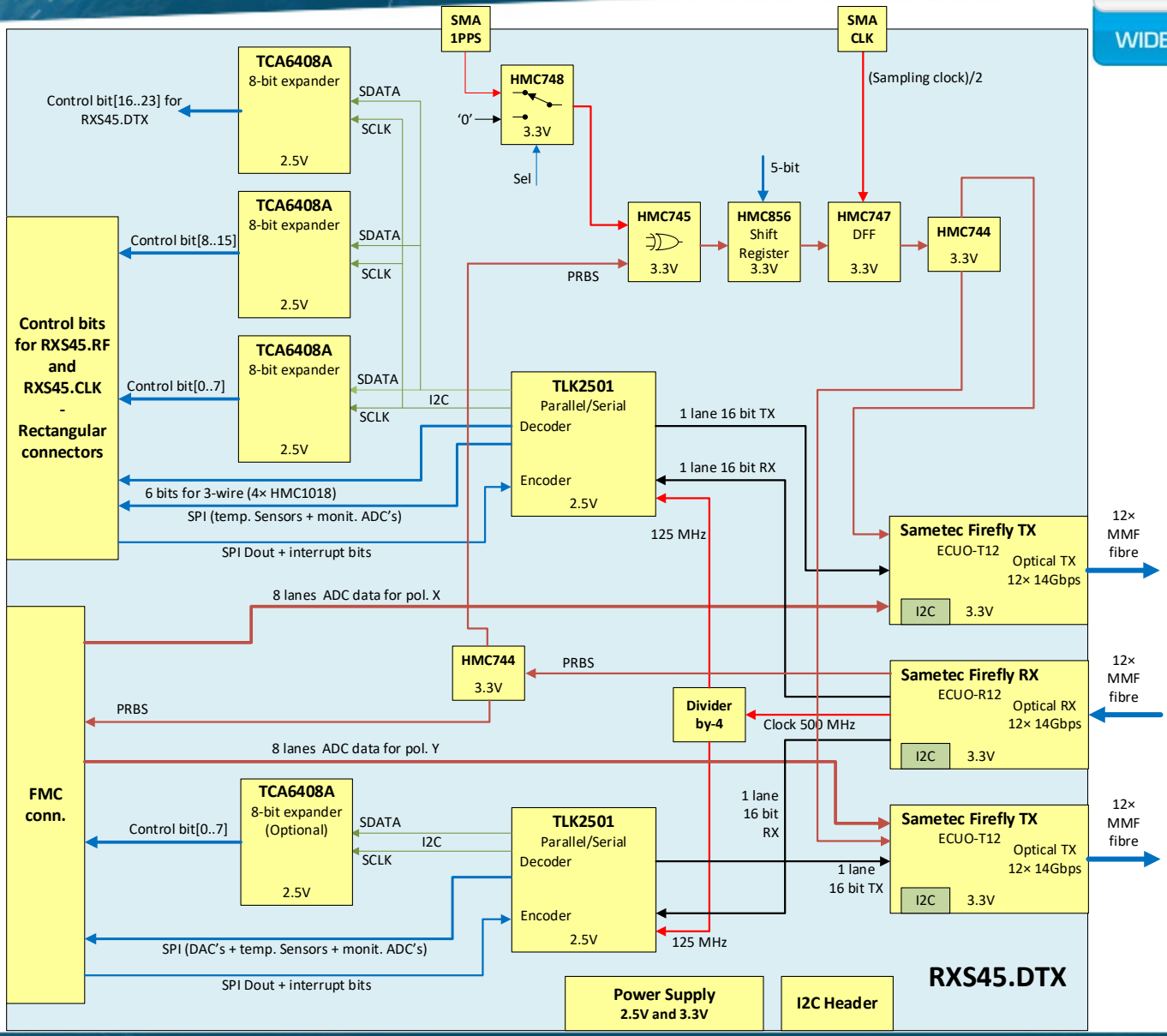


Data Transmission: RXS.DTX

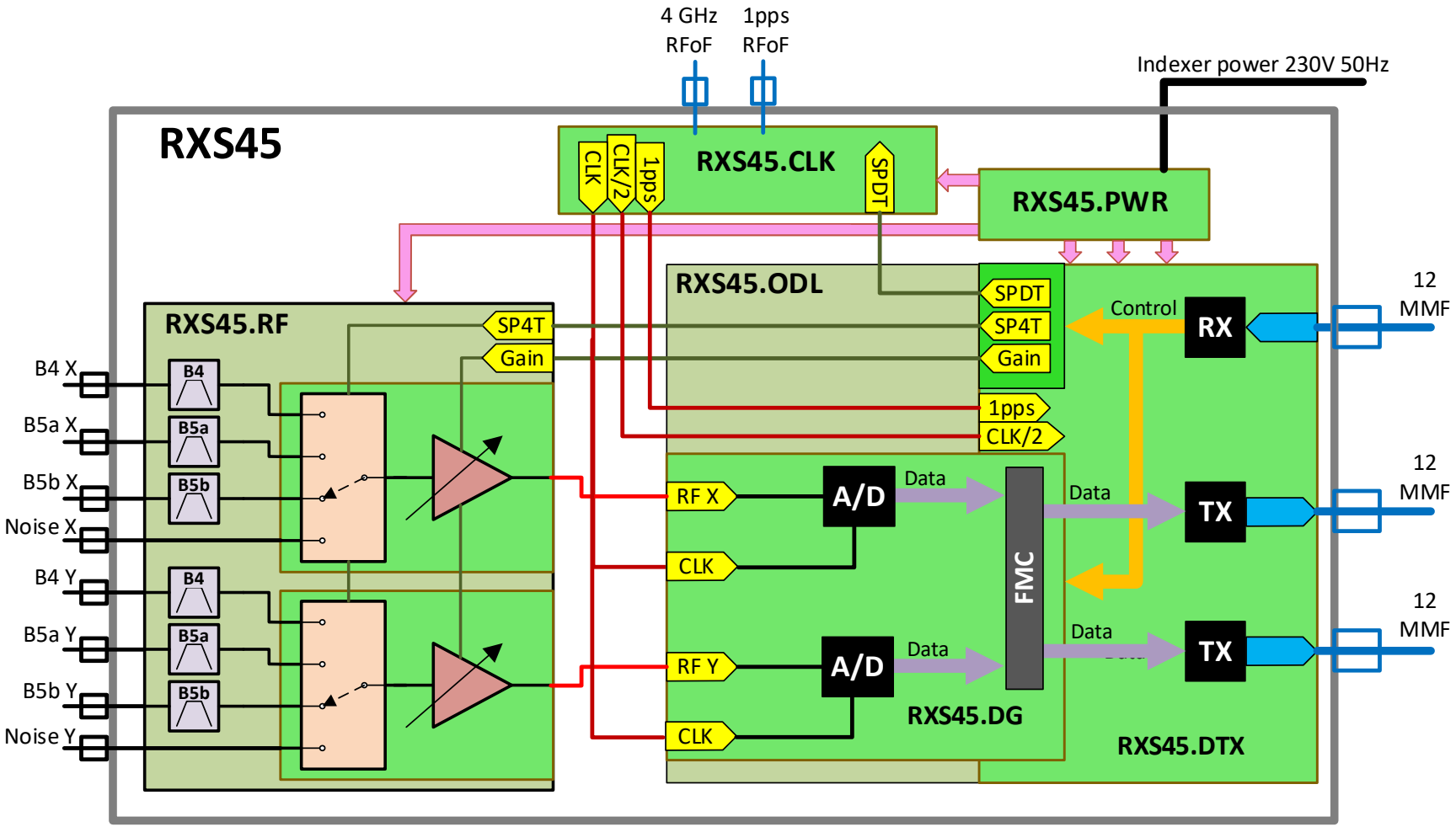
- The key components for ODL have been selected
  - Firefly optical system from Samtec (1 to 14 Gbps)
    - 2 × 12 TX channels for ADC data and monitoring signals
    - 12 RX channels for PRBS and control signals

  - Parallel to serial circuit at 2.5 Gbps for LMC signals
    - 1:20 deserialization with 8b10b decoding stage
    - 20:1 serialization with 8b10b encoding stage

Data Transmission: RXS.DTX

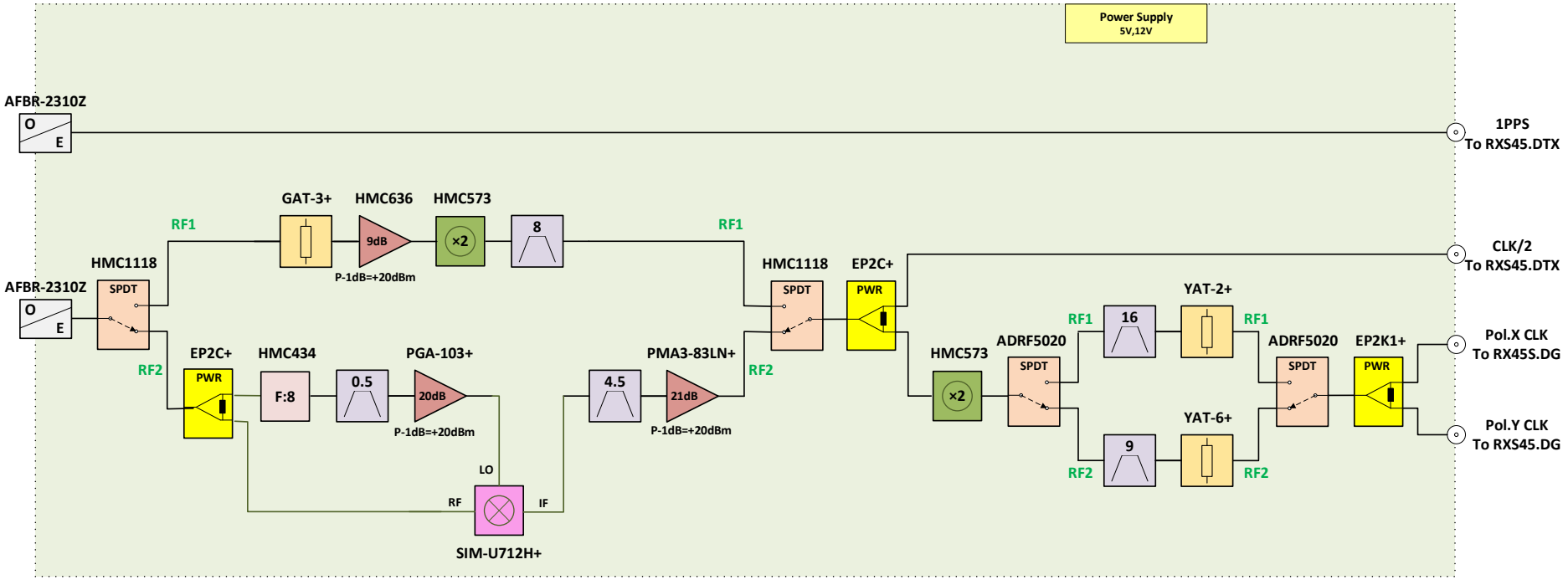


Receiver Part on Feed Indexer



Clock Conditioner Module: RXS45.CLK

- Sampling clocks for SKA1-MID
  - 16 GHz for Bands 4 and 5b sampling (and 5c- between 16.2 and 19.8 GHz)
  - 9 GHz for Band 5a sampling
- Surface mount devices (cost and size savings)

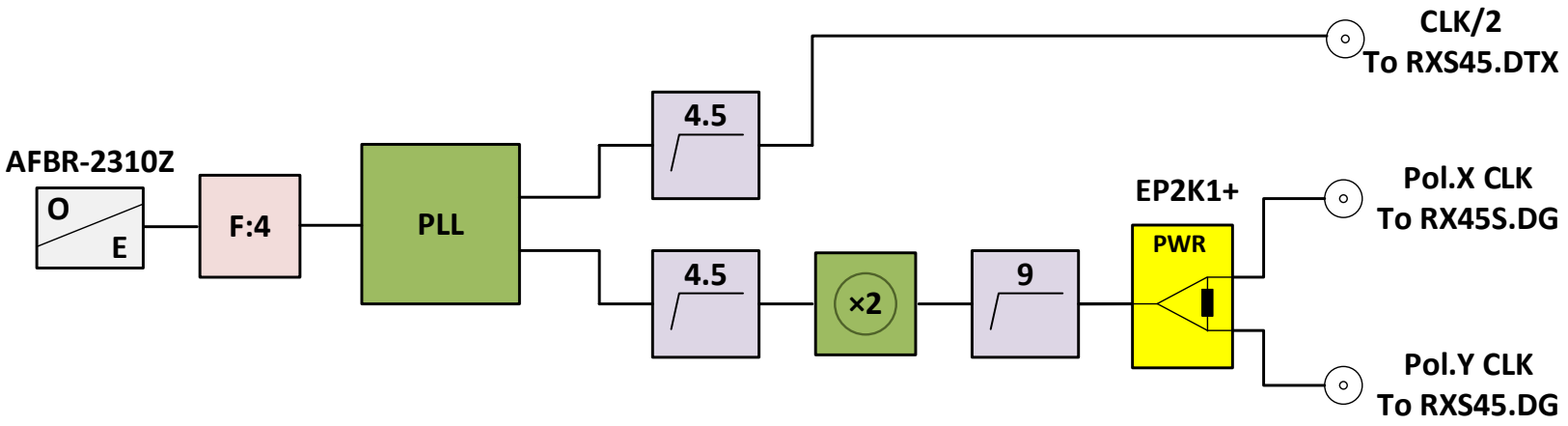


Clock Conditioner Module: RXS45.CLK

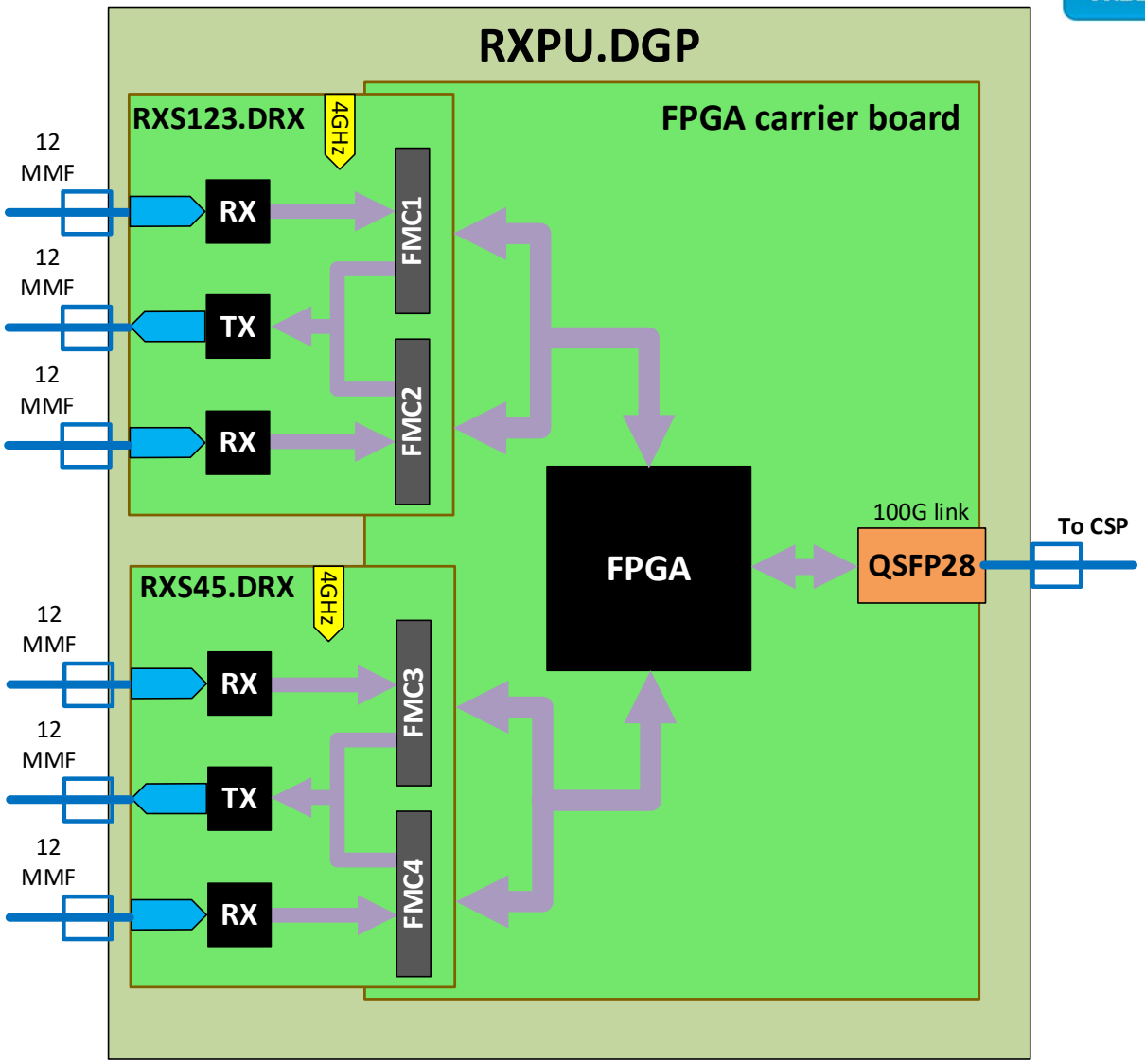
- Band 5 ECP (ECP160022)

	Freq. Range	Sampling clock	ADC output speed
Band 4	2.8 – 5.18 GHz	17 GHz	8.5 Gbps
Band 5a	5.0 – 9.25 GHz	9.5 GHz	4.75 Gbps
Band 5b	9 – 16.7 GHz	17 GHz	8.5 Gbps
Band 5c	16.4 – 24 GHz	16.2 GHz	8.1 Gbps

- PLL from TI: LMX2592 (9800 MHz max)

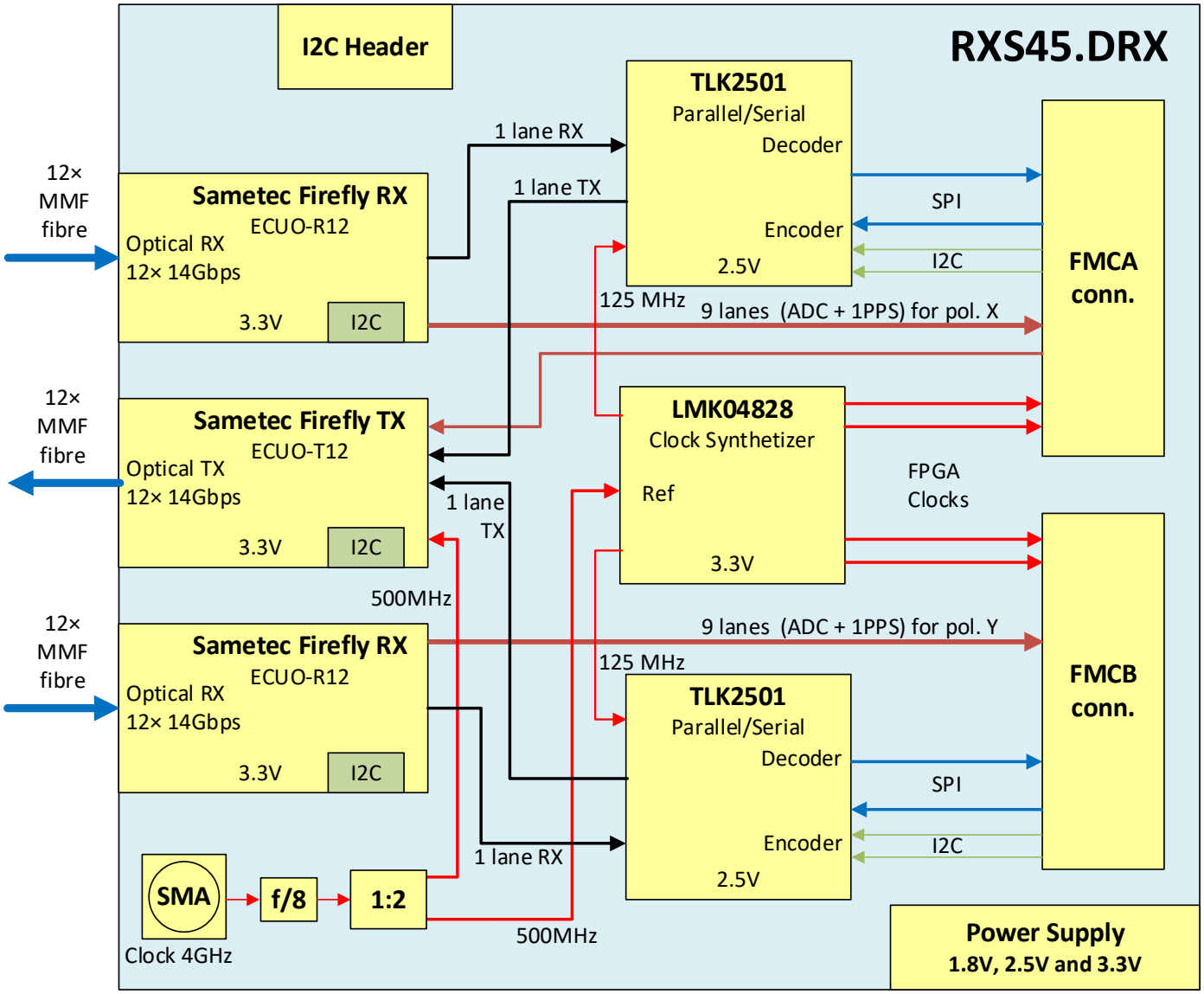


Part in Pedestal



Data Reception: RXS45.DRX

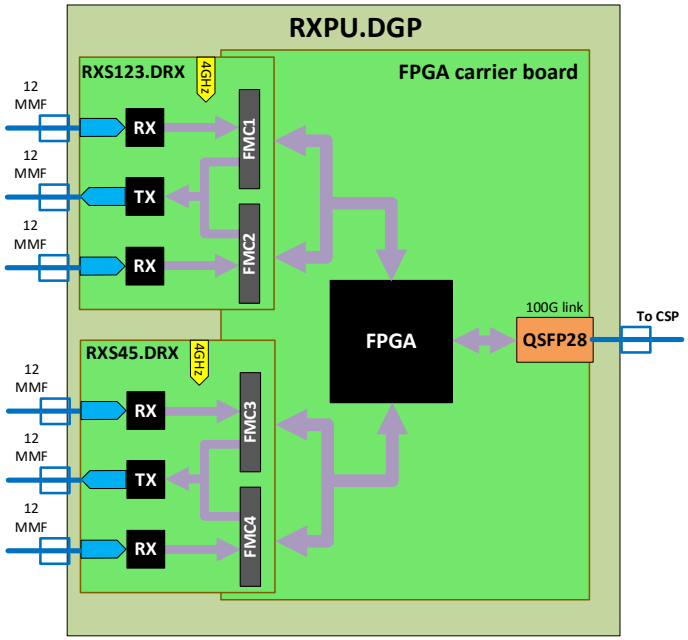
WIDE BAND SINGLE PIXEL FEEDS



FPGA Carrier Board

- Arria 10 Evalutation Kit from Altera
  - Digitizer characterization
  - Ripple/slope correction
  - Data transmission checking

- Custom board for deployement in more than 100 antenna
  - 4 FMC connectors for RXS123.DRX and RXS45.DRX
  - QSFP28 for 100G link
  - FPGA with sufficent logic ressources for Band 5b processing



Thank you